

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP6275SDSR

REVISION : 1.3

DATE : Mar. 29th , 2023

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		



正基科技股份有限公司



AP6275SDSR Data Sheet

Address:

8F., No.15-1, Zhonghua Rd., Hukou Township, Hsinchu County, Taiwan,
30352

Website:

<http://www.ampak.com.tw>



Revision

Revision	Date	Description	Revised By
0.1	2022/04/28	- Preliminary	Ali
0.2	2022/05/10	- Modify Pin Definition - Dimensions	Ali
1.0	2022/06/07	- Modify General Specification - Modify Wi-Fi Specification - Modify Bluetooth Specification	Ali
1.0	2022/06/07	- Modify General Specification	Ali
1.1	2022/10/15	- Modify Pin Definition	Ali
1.2	2023/02/05	- Dimension	Ali
1.3	2023/03/29	- Modify Introduction - Modify Wi-Fi Specification - Dimensions	Ali

Contents

1. Introduction	2
1.1 Overview.....	2
1.2 Product Features.....	3
2. General Specification	4
2.1 General Specification.....	4
2.2 DC Characteristics	4
2.2.1 Absolute Maximum Ratings.....	4
2.2.2 Recommended Operating Rating	5
3. Wi-Fi RF Specification.....	6
3.1 2.4GHz RF Specification	6
3.2 5GHz RF Specification	8
4. Bluetooth Specification	14
4.1 Bluetooth Specification.....	14
5. Pin Definition	15
5.1 Pin Outline	15
5.2 Pin Assignment	15
6. Dimensions	19
6.1 Module Dimensions	19
6.2 Recommended footprint.....	20
7. Host Interface Timing Diagram.....	22
7.1 Power-up Sequence Timing Diagram	22
7.2 SDIO Interface Description	24
7.3 PCM Interface Description	30
7.4 UART Interface Description	34
8. Recommended Reflow Profile	35
9. Package Information.....	36
9.1 Label.....	36
9.2 Dimension.....	37

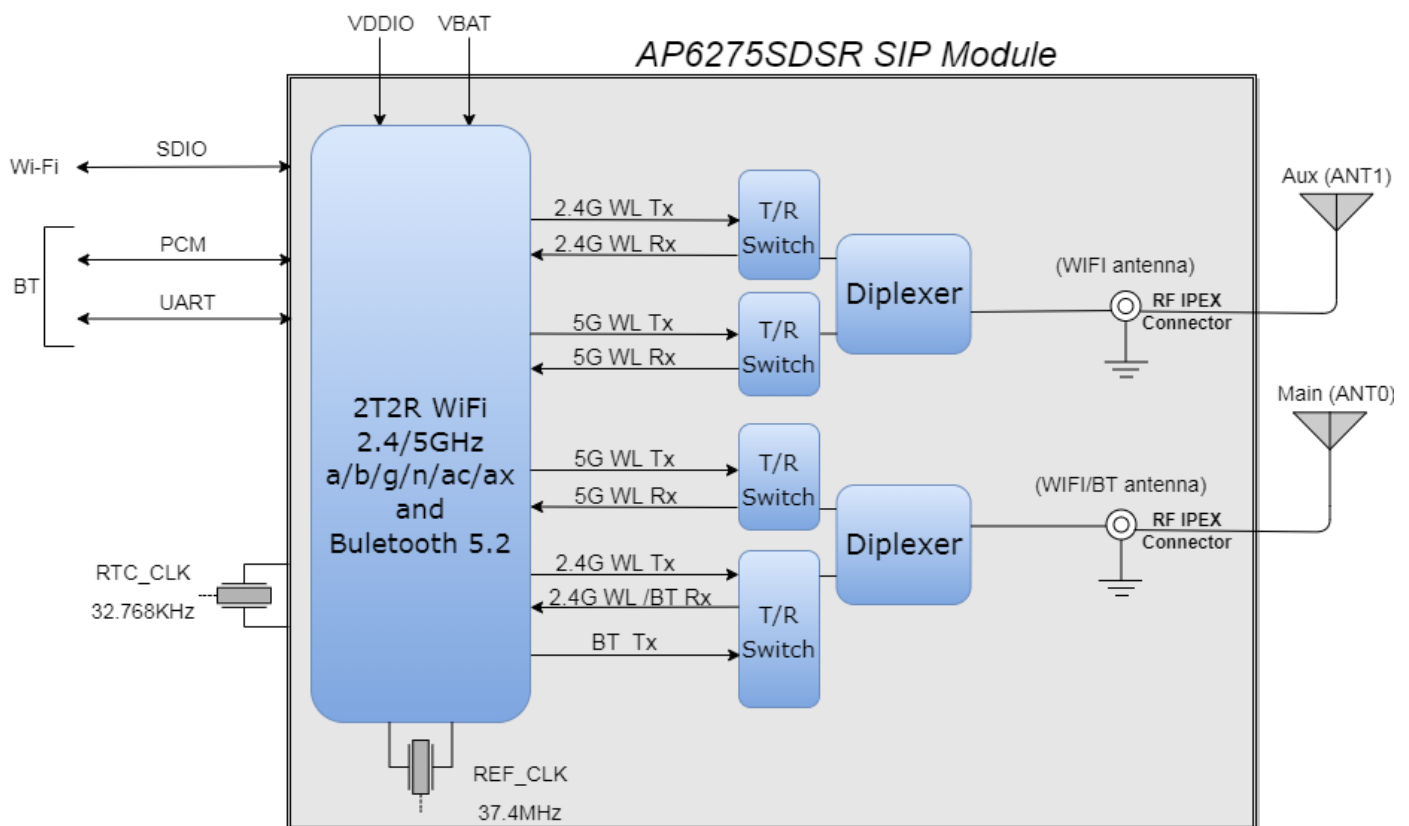


1. Introduction

1.1 Overview

The AMPAK Technology® AP6275SDSR is a fully Wi-Fi 6(2.4/5GHz) and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac 2x2 Access Points with MIMO standard and can accomplish up to speed of 1200Mbps with dual stream in 802.11ax to connect the wireless LAN. Furthermore AP6275SDSR included SDIO interface for Wi-Fi, UART/ PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

IEEE 802.11 Key Features

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 1200 Mbps data rate.
- 20/40/80 MHz channels for 5GHz and 6GHz (U-NII-5 and U-NII-6) radio, and 20MHz channels for 2.4GHz radio.
- Client MU-MIMO.
- Supports 2 antennas with two for shared BT and WLAN port.
- Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.

Bluetooth Key Features

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
 - Complies with Bluetooth Core Specification Version 5.2 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
 - Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
 - Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- A simplified block diagram of the module is depicted in the figure above.
- BT Core Specification Version 5.2, including the following support:
 - Low energy(LE) isochronous channels
 - LE power control
 - LE enhanced connection update
 - LE channel classification
 - LE audio

2. General Specification

2.1 General Specification

Model Name	AP6275SDSR
Product Description	2T2R 802.11 ax/ac/a/b/g/n Wi-Fi 6 + BT 5.2 Module
Dimension	L x W: 12 x 16(typical) mm H: 1.8(Maximum) mm
WiFi Interface	Support SDIO V3.0/2.0
BT Interface	UART / PCM
Operating temperature	-40°C to +85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.6V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/ Bluetooth/ I/O Voltage	-0.5	2.07	V

IC ESD SPEC: Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	IC ESD Specification Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1.5	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	300 ^a	V

a. 250V for BT_13DBMOP and BT_PAVDD_V3P3.

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	4.8	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIH	$0.65 \times VDDIO$	N/A	V
VIL	N/A	$0.4 \times VDDIO$	V
VOH output@2mA	$VDDIO - 0.4$	N/A	V
VOL output@2mA	N/A	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11b/g/n/ax & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11 g/n：OFDM_64-QAM、16-QAM、QPSK、BPSK 802.11ax：OFDM_256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	19	19	18.5	18.5	18
	54Mbps				
	16.5				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	19	18.5	18.5	18	16.5
	MCS7				
	16				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	19	18.5	18.5	18	16.5
	HE7	HE8	HE9		
	16	16	15		
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER ≤ 8%、OFDM modulation PER ≤ 10%					
802.11b	Data Rate	Spec.(dBm)			
	1Mbps	-97			
	2Mbps	-93			
	5.5Mbps	-91			
	11Mbps	-88			

802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92.5	24Mbps	-84.5
	9Mbps	-91.5	36Mbps	-81.5
	12Mbps	-90.5	48Mbps	-78
	18Mbps	-87.5	54Mbps	-75.5
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-95	24Mbps	-87
	9Mbps	-94	36Mbps	-84
	12Mbps	-93	48Mbps	-81
	18Mbps	-90	54Mbps	-78
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS4	-81.5
	MCS1	-89	MCS5	-78
	MCS2	-87	MCS6	-75.5
	MCS3	-84	MCS7	-74.5
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS5	-80
	MCS1	-92	MCS6	-78
	MCS2	-90	MCS7	-76
	MCS3	-87	MCS8	-72
	MCS4	-83	MCS15	-73
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-92	HE6	-75.5
	HE1	-89	HE7	-74.5
	HE2	-87	HE8	-72
	HE3	-84	HE9	-70
	HE4	-81.5		
	HE5	-78		
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac/ax & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz （5GHz UNII Band）			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch140 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM_64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM_64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM_256-QAM 、 OFDM_64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ax ： OFDM_1024-QAM、 OFDM_256-QAM、OFDM_64-QAM、16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	15.5	15		
	5470~5720	15.5	15		
	5725~5845	15.5	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14		
	5470~5720	15	14		
	5725~5845	15	14		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15	15
	5470~5720	15.5	15.5	15	15
	5725~5845	15.5	15.5	15	15
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	14.5	13.5		
	5470~5720	14.5	13.5		
	5725~5845	14.5	13.5		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15	14	11.5	
	5470~5720	15	14	11.5	
	5725~5845	15	14	11.5	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5720	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14.5	14	11.5	10
	5470~5720	14.5	14	11.5	10
	5725~5845	14.5	14	11.5	10
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15	14.5	14.5
	5470~5720	15.5	15	14.5	14.5
	5725~5845	15.5	15	14.5	14.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14	14	10	10
	5470~5720	14	14	10	10
	5725~5845	14	14	10	10

802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	16	15.5	15.5	15.5
	5470~5720	16	15.5	15.5	15.5
	5725~5845	16	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	14.5	14.5	11.5	11.5
	5470~5720	14.5	14.5	11.5	11.5
	5725~5845	14.5	14.5	11.5	11.5
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5720	10	10		
	5725~5845	10	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15	15	15	15
	5470~5720	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	14.5	14	12	10
	5470~5720	14.5	14	12	10
	5725~5845	14.5	14	12	10
	Frequency (MHz)	HE10	HE11		
	5150~5350	8	8		
	5470~5720	8	8		
	5725~5845	8	8		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15	14.5	14.5
	5470~5720	15.5	15	14.5	14.5
	5725~5845	15.5	15	14.5	14.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	14	14	10	10
	5470~5720	14	14	10	10
	5725~5845	14	14	10	10
	Frequency (MHz)	HE10	HE11		
	5150~5350	8	8		
	5470~5720	8	8		
	5725~5845	8	8		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB
OFDM modulation PER $\leq 10\%$

802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-89	24Mbps	-82
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-75
	18Mbps	-86	54Mbps	-72
MIMO802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-85
	9Mbps	-91	36Mbps	-83
	12Mbps	-90	48Mbps	-78
	18Mbps	-89	54Mbps	-75
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS4	-78
	MCS1	-87	MCS5	-75
	MCS2	-86	MCS6	-72
	MCS3	-82	MCS7	-70
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
	MCS1	-90	MCS6	-75
	MCS2	-88	MCS7	-73
	MCS3	-85	MCS8	-88
	MCS4	-81	MCS15	-69
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS4	-76
	MCS1	-85	MCS5	-71
	MCS2	-82	MCS6	-70
	MCS3	-79	MCS7	-68
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-71
	MCS3	-83	MCS8	-86
	MCS4	-79	MCS15	-67

802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS5	-74
	MCS1	-87	MCS6	-72
	MCS2	-86	MCS7	-70
	MCS3	-82	MCS8	-67
	MCS4	-78		
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-92	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-72
	MCS2,NSS=1	-87	MCS8,NSS=1	-70
	MCS3,NSS=1	-84	MCS0,NSS=2	-88
	MCS4,NSS=1	-81	MCS8,NSS=2	-65
	MCS5,NSS=1	-77		
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS5	-71
	MCS1	-85	MCS6	-69
	MCS2	-82	MCS7	-68
	MCS3	-79	MCS8	-64
	MCS4	-75	MCS9	-63
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-89.5	MCS6,NSS=1	-71.5
	MCS1,NSS=1	-87.5	MCS7,NSS=1	-70.5
	MCS2,NSS=1	-84.5	MCS8,NSS=1	-66.5
	MCS3,NSS=1	-81.5	MCS9,NSS=1	-65.5
	MCS4,NSS=1	-77.5	MCS0,NSS=2	-85.5
	MCS5,NSS=1	-73.5	MCS9,NSS=2	-59.5
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-84	MCS5	-67
	MCS1	-81	MCS6	-65
	MCS2	-78	MCS7	-63
	MCS3	-75	MCS8	-62
	MCS4	-72	MCS9	-60

802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-87	MCS6,NSS=1	-68
	MCS1,NSS=1	-84	MCS7,NSS=1	-66
	MCS2,NSS=1	-81	MCS8,NSS=1	-65
	MCS3,NSS=1	-78	MCS9,NSS=1	-63
	MCS4,NSS=1	-75	MCS0,NSS=2	-83
	MCS5,NSS=1	-70	MCS9,NSS=2	-58
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-89	HE6	-72
	HE1	-87	HE7	-69
	HE2	-86	HE8	-67
	HE3	-82	HE9	-63
	HE4	-78	HE10	-58
	HE5	-74	HE11	-55
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-87	HE6	-69
	HE1	-85	HE7	-68
	HE2	-82	HE8	-64
	HE3	-79	HE9	-63
	HE4	-75	HE10	-59
	HE5	-71	HE11	-54
802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-84	HE6	-67
	HE1	-81	HE7	-65
	HE2	-78	HE8	-62
	HE3	-75	HE9	-60
	HE4	-72	HE10	-55
	HE5	-67	HE11	-51
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

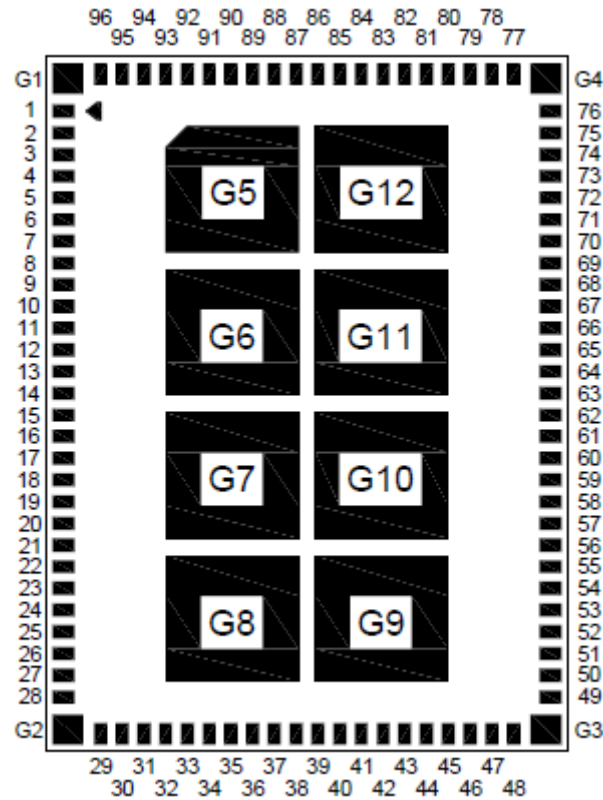
Feature	Description
General Specification	
Bluetooth Standard	BDR 、EDR(2 、3Mbps) 、LE(1Mbps) 、LE2(2Mbps) 、LELR
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic 、40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 2.5 dB	
	CL1 (dBm)
BDR Output Power	7
EDR Output Power	5
BLE Output Power	7
Sensitivity, tolerance ± 2 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-89 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-92 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-92 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-91 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Assignment

NO	Name	Type	Description
1	NC	—	Floating (Don't connected to ground)
2	NC	—	Floating (Don't connected to ground)
3	WL_GPIO4	I/O	WLAN GPIO 4
4	VBAT	I	VBAT system power supply input
5	VBAT	I	VBAT system power supply input
6	GND	—	Ground connections
7	WL_GPIO5	I/O	WLAN GPIO 5
8	WL_GPIO8	I/O	WLAN GPIO 8
9	WL_GPIO9	I/O	WLAN GPIO 9
10	NC	—	Floating (Don't connected to ground)
11	NC	—	Floating (Don't connected to ground)
12	ABUCK_1P12	I	Internal Buck voltage generation pin
13	ABUCK_1P12	I	Internal Buck voltage generation pin

14	GND	—	Ground connections
15	ASR_VLX	O	Internal Analog Buck voltage generation pin
16	ASR_VLX	O	Internal Analog Buck voltage generation pin
17	GND	—	Ground connections
18	CSR_VLX	O	Internal Analog Buck voltage generation pin
19	CSR_VLX	O	Internal Analog Buck voltage generation pin
20	GND	—	Ground connections
21	CBUCK_OP9	I	Internal Buck voltage generation pin
22	CBUCK_OP9	I	Internal Buck voltage generation pin
23	GND	—	Ground connections
24	BT_WAKE	I	HOST wake-up Bluetooth device
25	NC	—	Floating (Don't connected to ground)
26	GND	—	Ground connections
27	LPO_IN	I	External Low Power Clock input (32.768KHz)
28	WL_GPIO1	I/O	WLAN GPIO 1/WL_DEV_WAKE
29	NC	—	Floating (Don't connected to ground)
30	NC	—	Floating (Don't connected to ground)
31	NC	—	Floating (Don't connected to ground)
32	GND	—	Ground connections
33	NC	—	Floating (Don't connected to ground)
34	NC	—	Floating (Don't connected to ground)
35	GND	—	Ground connections
36	NC	—	Floating (Don't connected to ground)
37	NC	—	Floating (Don't connected to ground)
38	GND	—	Ground connections
39	NC	—	Floating (Don't connected to ground)
40	NC	—	Floating (Don't connected to ground)
41	GND	—	Ground connections
42	NC	—	Floating (Don't connected to ground)
43	NC	—	Floating (Don't connected to ground)
44	NC	—	Floating (Don't connected to ground)
45	WL_REG_ON	I	Low asserting reset for WiFi core
46	WL_HOST_WAKE	O	WLAN to wake-up HOST
47	SDIO_DATA_3	I/O	SDIO data line 3
48	SDIO_DATA_2	I/O	SDIO data line 2
49	SDIO_DATA_1	I/O	SDIO data line 1
50	SDIO_DATA_0	I/O	SDIO data line 0
51	SDIO_DATA_CMD	I/O	SDIO command line
52	SDIO_DATA_CLK	I/O	SDIO clock line

53	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
54	BT_UART_CTS	I	Bluetooth UART clear to send
55	BT_UART_TX	O	Bluetooth UART serial data output
56	BT_UART_RX	I	Bluetooth UART serial data input
57	BT_UART_RTS	O	Bluetooth UART request to send
58	PCM_SYNC	I/O	PCM Sync; can be master (output) or slave (input)
59	PCM_IN	I	PCM data input
60	PCM_OUT	O	PCM Data output
61	PCM_CLK	I/O	PCM clock; can be master (output) or slave (input)
62	GND	—	Ground connections
63	BT_REG_ON	I	Low asserting reset for Bluetooth core
64	WL_GPIO2	I/O	WLAN GPIO 2
65	WL_GPIO3	I/O	WLAN GPIO 3
66	DBG_UART_RX/WL_GPIO10	I/O	DBG UART Tx , WLAN GPIO 10
67	DBG_UART_TX/WL_GPIO11	I/O	DBG UART Rx , WLAN GPIO 11
68	GND	—	Ground connections
69	NC	—	Floating (Don't connected to ground)
70	NC	—	Floating (Don't connected to ground)
71	GND	—	Ground connections
72	VIO	P	I/O 1.8 Voltage supply input
73	VIO	P	I/O 1.8 Voltage supply input
74	GND	—	Ground connections
75	GND	—	Ground connections
76	GND	—	Ground connections
77	GND	—	Ground connections
78	GND	—	Ground connections
79	GND	—	Ground connections
80	GND	—	Ground connections
81	GND	—	Ground connections
82	GND	—	Ground connections
83	GND	—	Ground connections
84	GND	—	Ground connections
85	GND	—	Ground connections
86	GND	—	Ground connections
87	GND	—	Ground connections
88	GND	—	Ground connections
89	GND	—	Ground connections
90	GND	—	Ground connections
91	GND	—	Ground connections

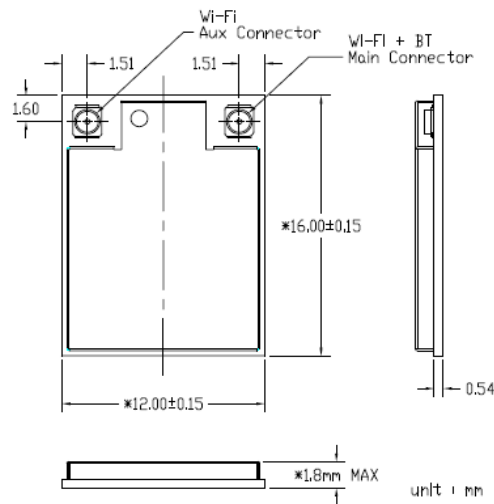
92	GND	—	Ground connections
93	GND	—	Ground connections
94	GND	—	Ground connections
95	GND	—	Ground connections
96	GND	—	Ground connections
G1	GND	—	Ground connections
G2	GND	—	Ground connections
G3	GND	—	Ground connections
G4	GND	—	Ground connections
G5	GND	—	Ground connections
G6	GND	—	Ground connections
G7	GND	—	Ground connections
G8	GND	—	Ground connections
G10	GND	—	Ground connections
G11	GND	—	Ground connections
G12	GND	—	Ground connections

6. Dimensions

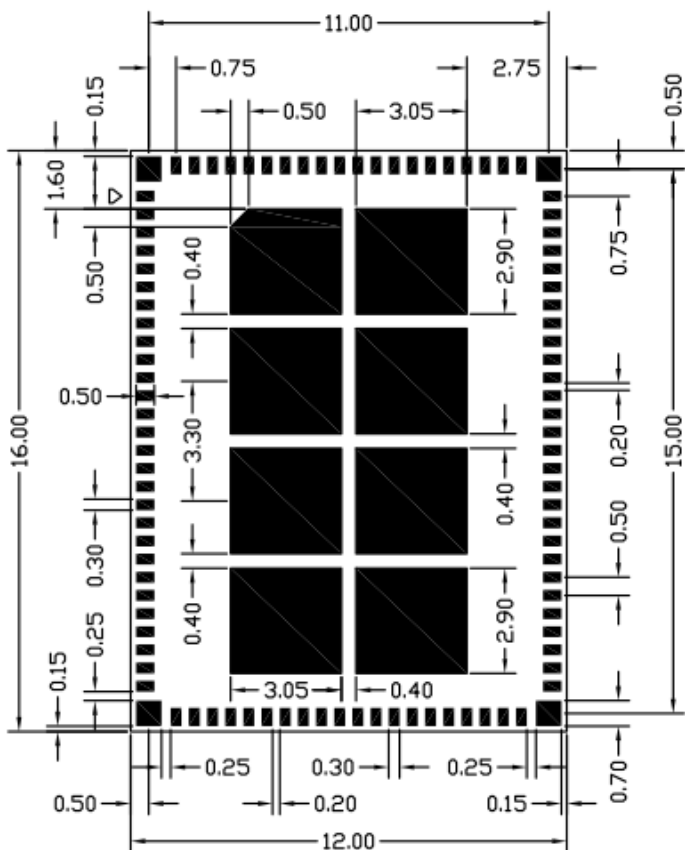
6.1 Module Dimensions

(Unit: mm)

< TOP VIEW >



< TOP VIEW >

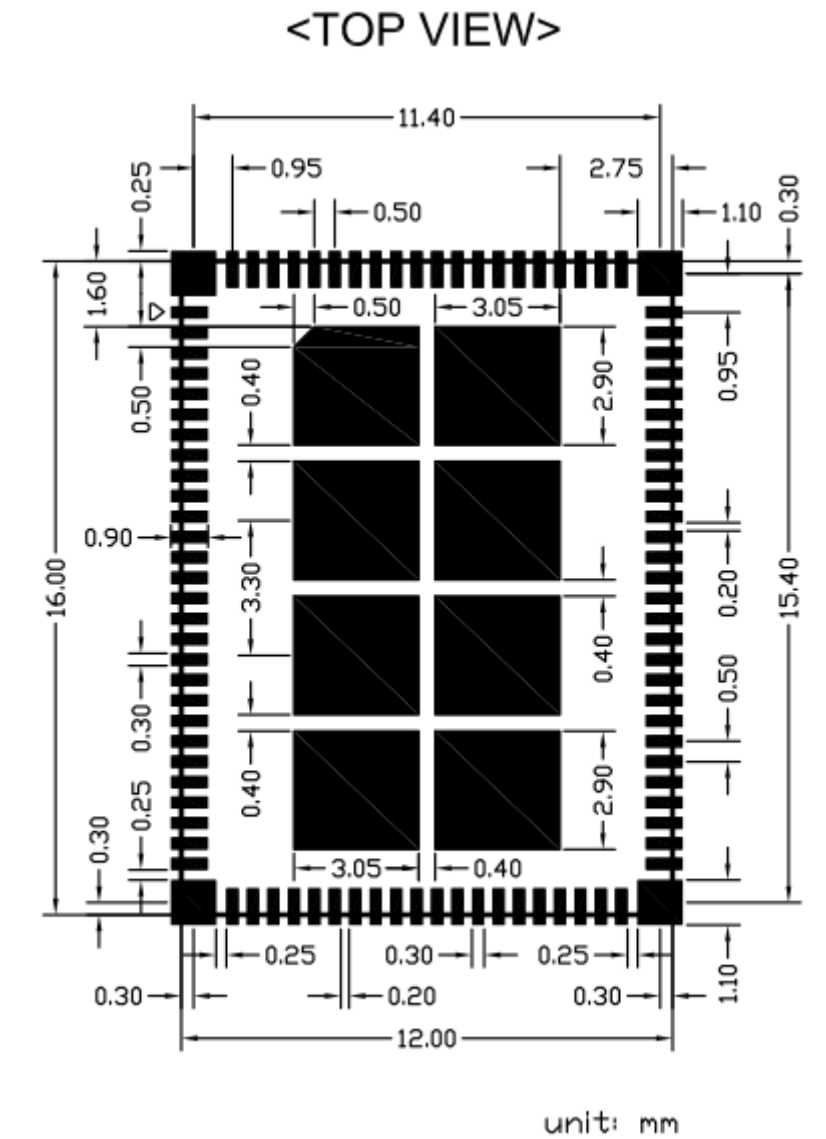


GENERAL TOLERANCE IS $\pm 0.10\text{mm}$
UNLESS OTHERWISE SPECIFIED

unit: mm

6.2 Recommended footprint

(Unit: mm)



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).

External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

7. Host Interface Timing Diagram

7.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- **WL_REG_ON**: This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the **BT_REG_ON** input to control the internal regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If **BT_REG_ON** and **WL_REG_ON** are both low, the regulators are disabled.
- **BT_REG_ON**: This signal is used by the PMU to decide whether or not to power down the internal regulators. If **BT_REG_ON** and **WL_REG_ON** are low, the regulators will be disabled.
- It suggests customers connect **WL_REG_ON** and **BT_REG_ON** to GPIOs for control, otherwise unexpected errors may occur when boot-up the device.
- In the figure, The **VDDIO** power supply has been included in the module. When **VBAT** is power-up, **VDDIO** will rise to high level after 15 ms.
- The module main chip has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after **VDDC** and **VDDIO** have both passed the POR threshold. Wait at least 150 ms after **VDDC** and **VDDIO** are available before initiating PCIe accesses.

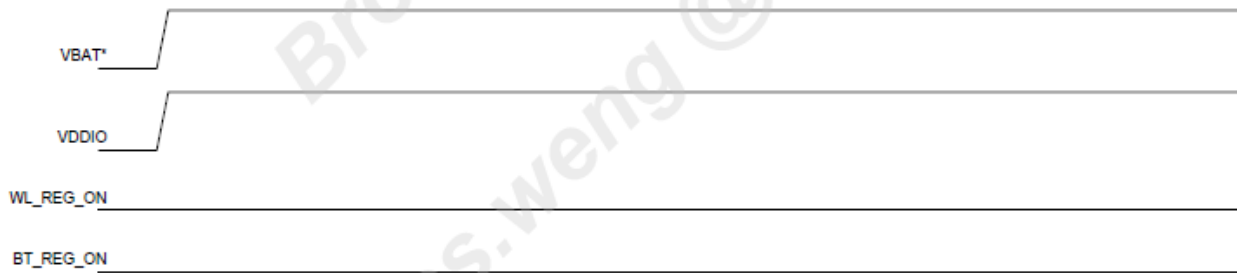


***Notes:**

1. The **VBAT** and **VDDIO** 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. **VBAT** should be up before or at the same time as **VDDIO**. **VDDIO** should NOT be present first or be held high before **VBAT** is high.

WLAN=ON, Bluetooth=ON

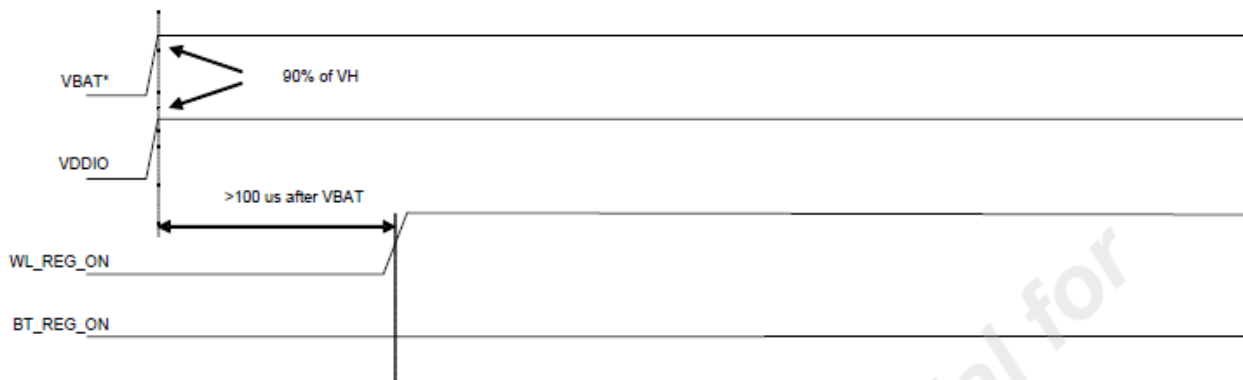




***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

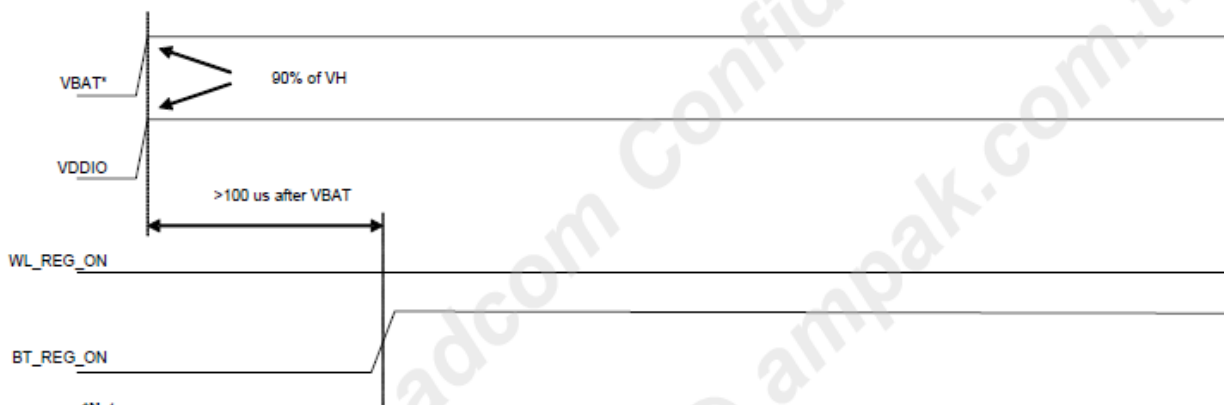
WLAN=OFF, Bluetooth=OFF



***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=OFF



***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=ON

7.2 SDIO Interface Description

The module WLAN section provides support for SDIO version 3.0 at 1.8V signaling, including the new UHS-1 mode:

DS : Default speed (DS) up to 25MHz, including 1- and 4-bit modes.

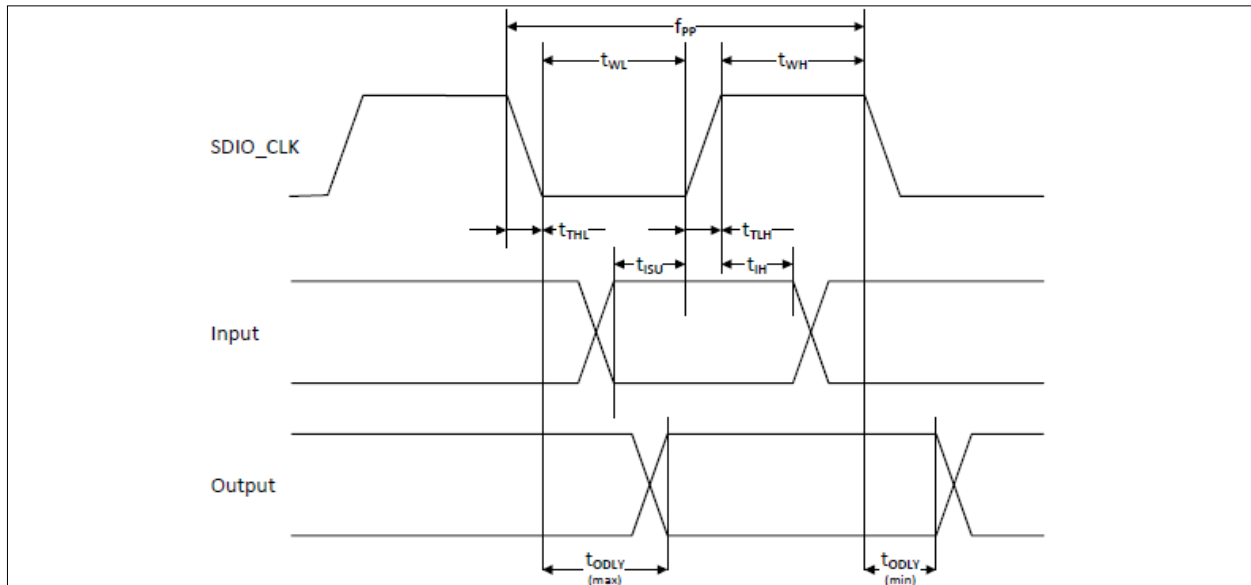
- SDR12 : SDR up to 25 MHz
- SDR25 : SDR up to 50MHz
- SDR50 : SDR up to 100MHz
- SDR104 : SDR up to 208MHz
- DDR50 : DDR up to 50MHz

Noted : The AP6275SDSR is backward compatible with SDIO V2.0 host interfaces.

SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode	
DATA0	Data Line 0	DATA	Data line
DATA1	Data Line 1 or Interrupt	IRQ	Interrupt
DATA2	Data Line 2 or Read Wait	RW	Read Wait
DATA3	Data Line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command Line	CMD	Command Line

SDIO Default Mode Timing Diagram



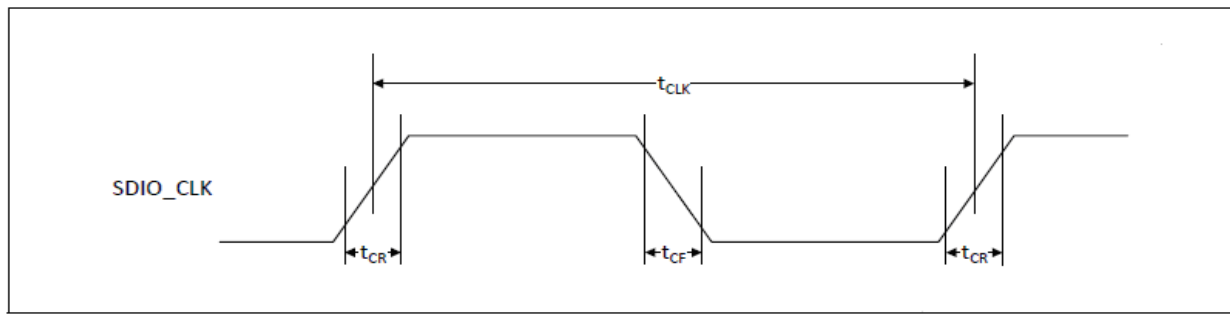
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

a. Timing is based on $CL \leq 40pF$ load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

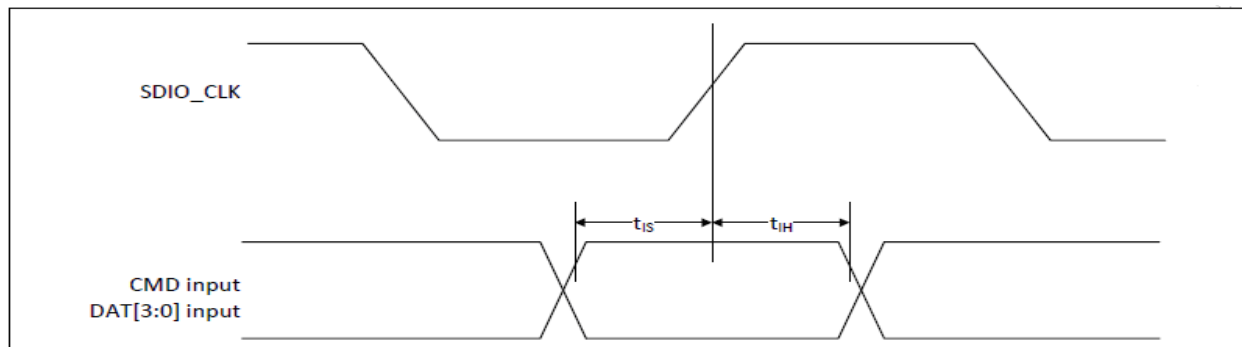
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



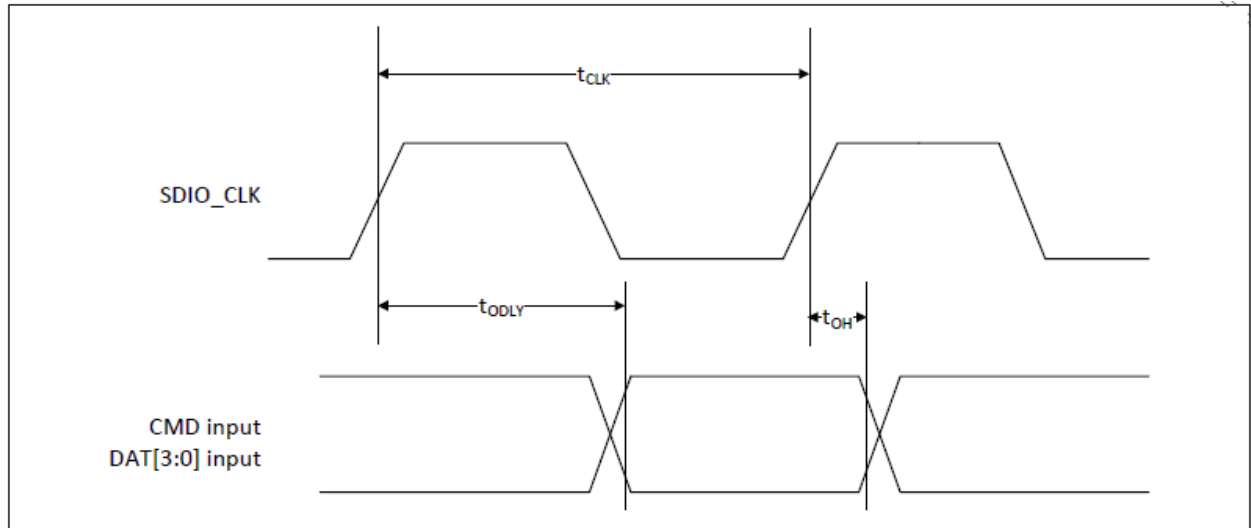
Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	–	30	70	%	–

SDIO Bus Input timing (SDR Modes)



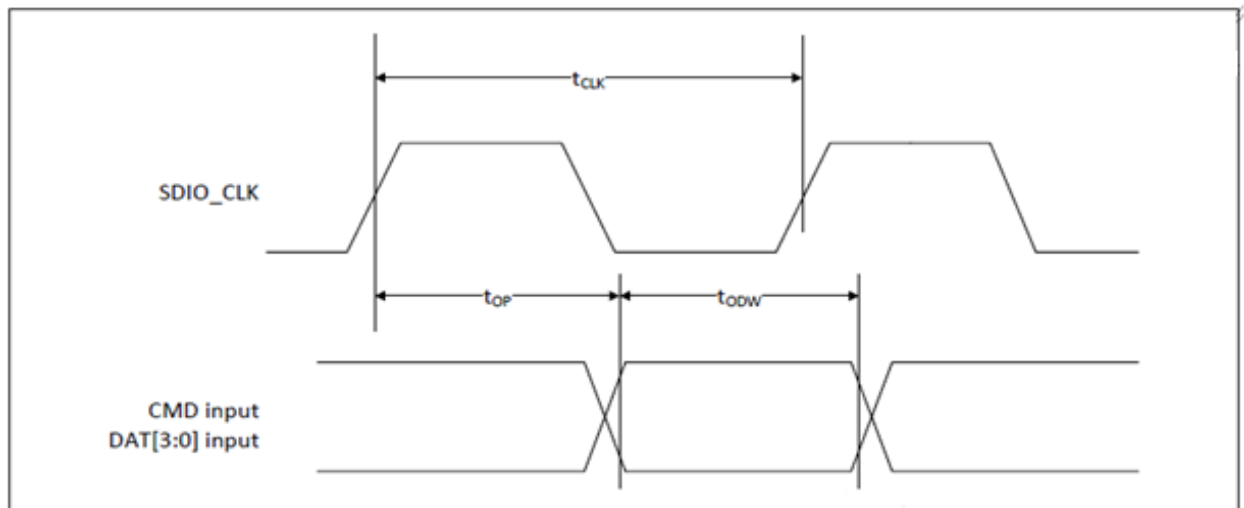
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

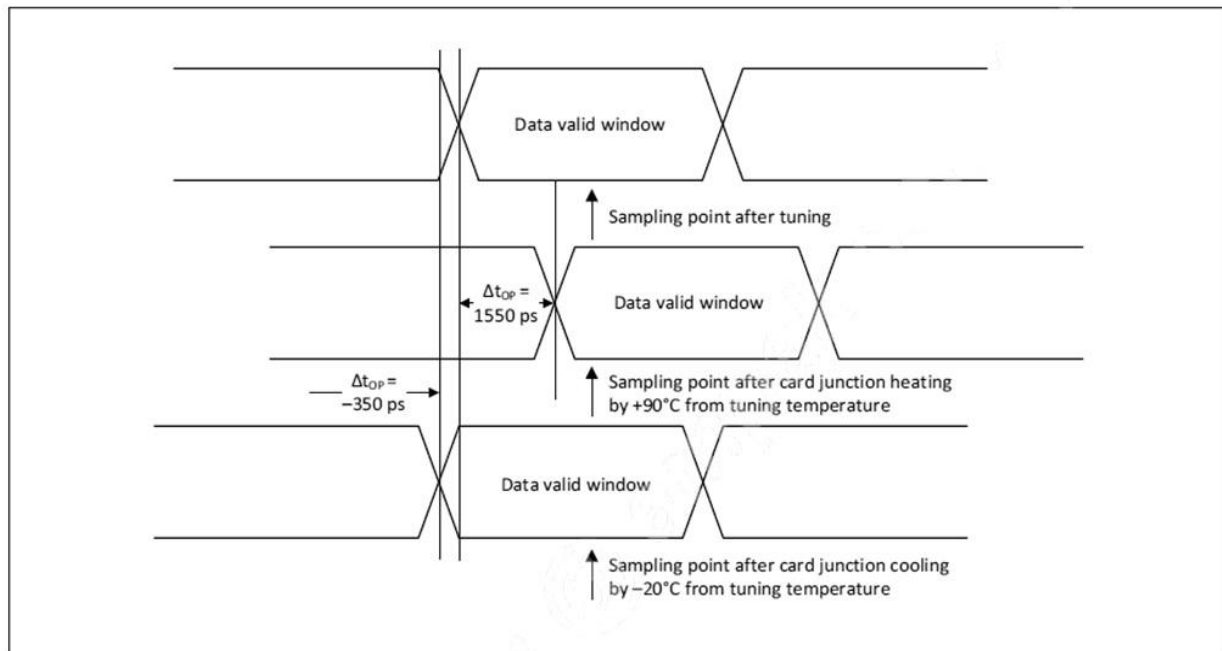
Card output timing (SDR Modes 100MHz to 208MHz)



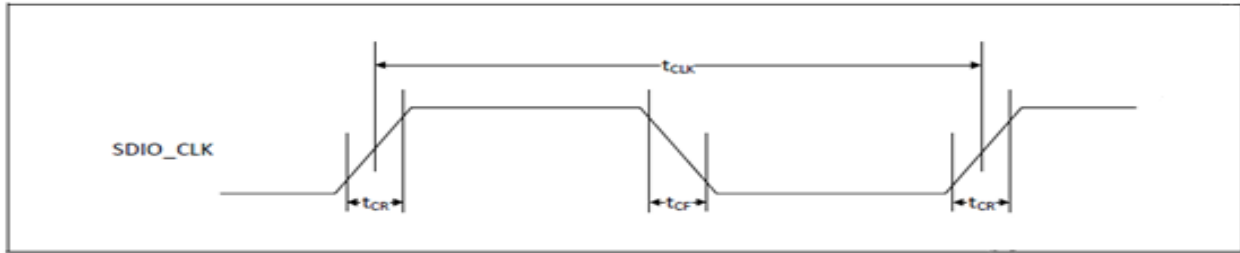
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	—	UI	$t_{ODW}=2.88$ ns @208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

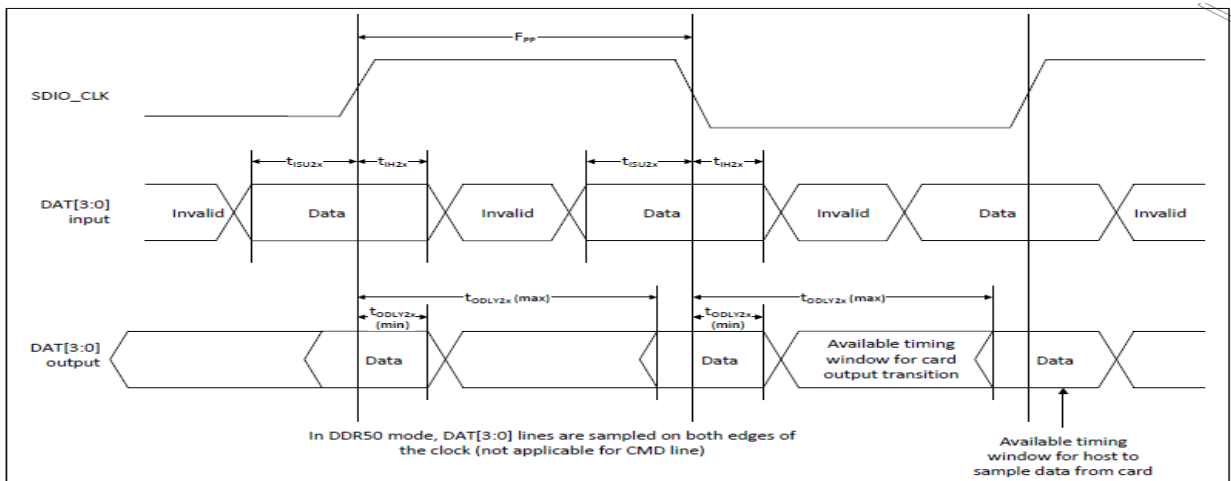


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	—	45	55	%	—

Data Timing



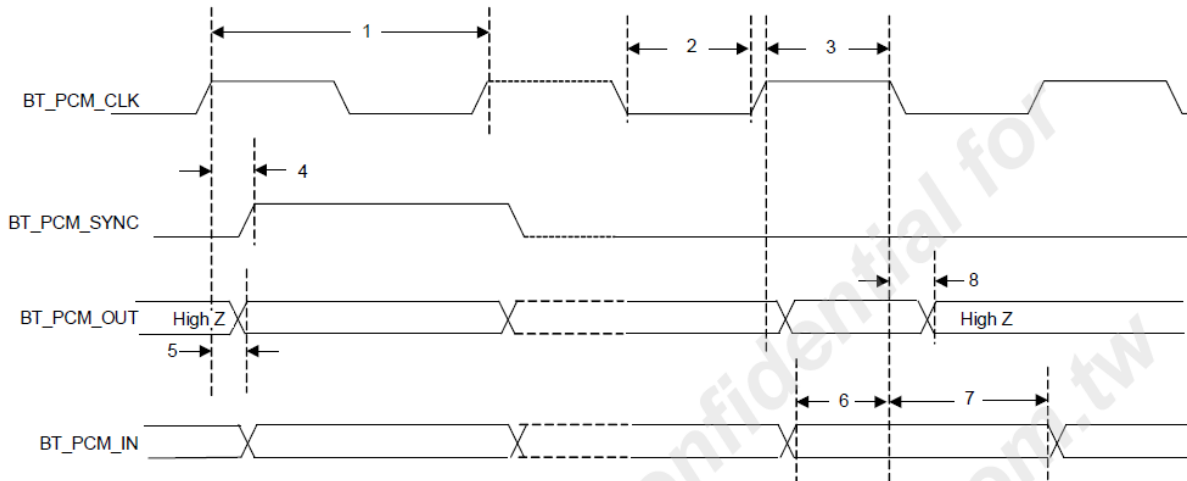
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30$ pF (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25$ pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)

7.3 PCM Interface Description

AP6275SDSR supports two independent PCM interfaces that share the pins with the I²S interfaces. The PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6275SDSR.

PCM Timing

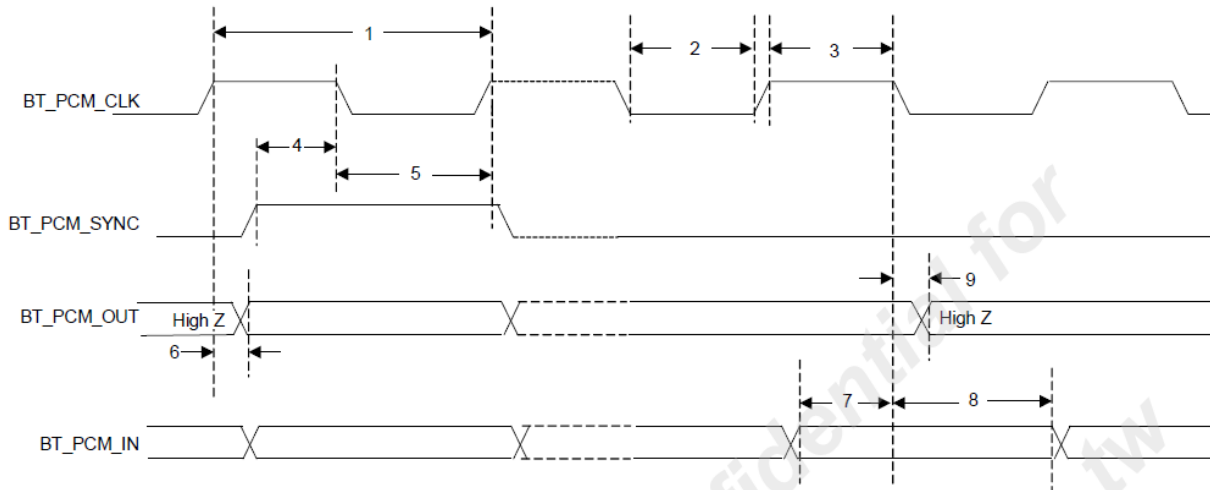
Short Frame Sync, Master Mode



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

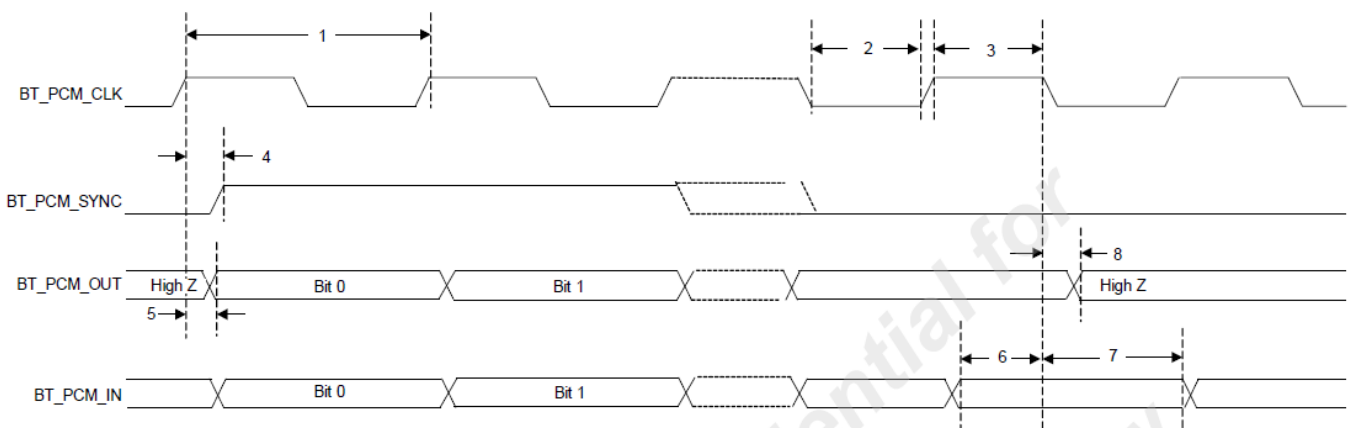


Short Frame Sync, Slave Mode



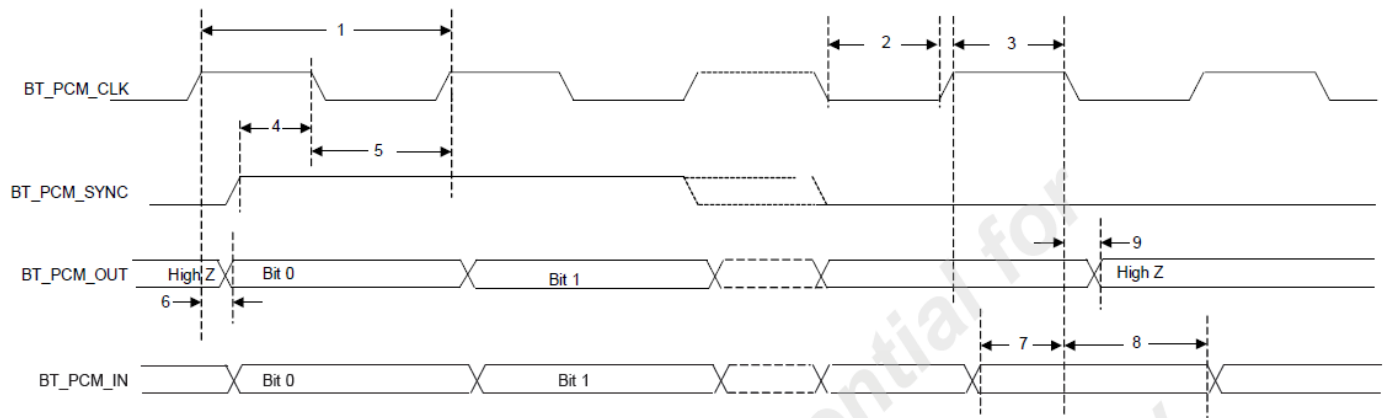
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

Long Frame Sync, Master Mode



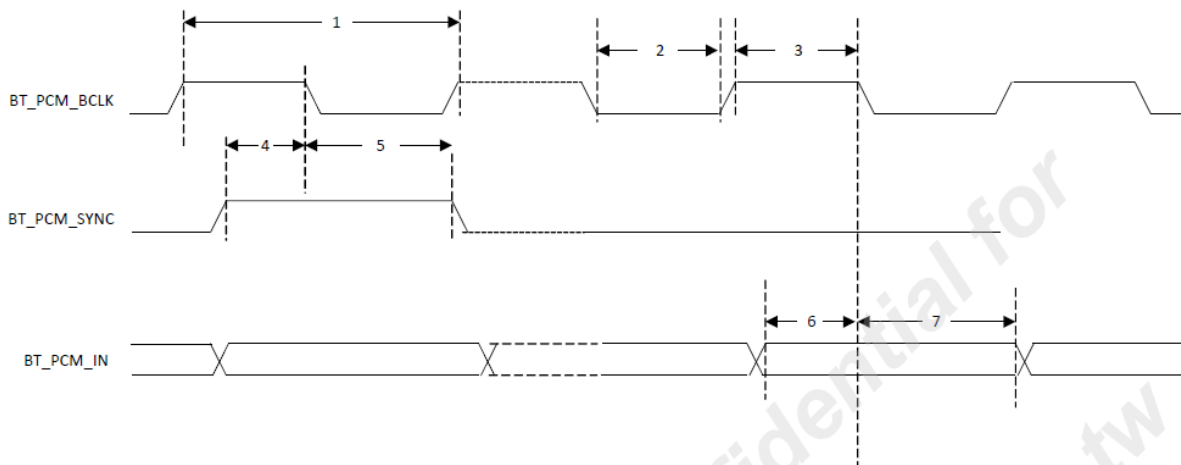
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

Long Frame Sync, Slave Mode



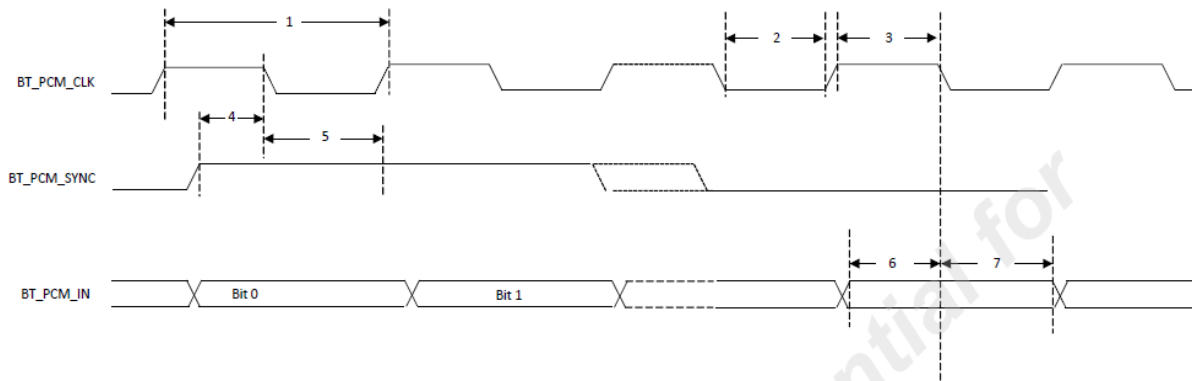
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

Short Frame Sync, Burst Mod



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns

Long Frame Sync, Burst Mode

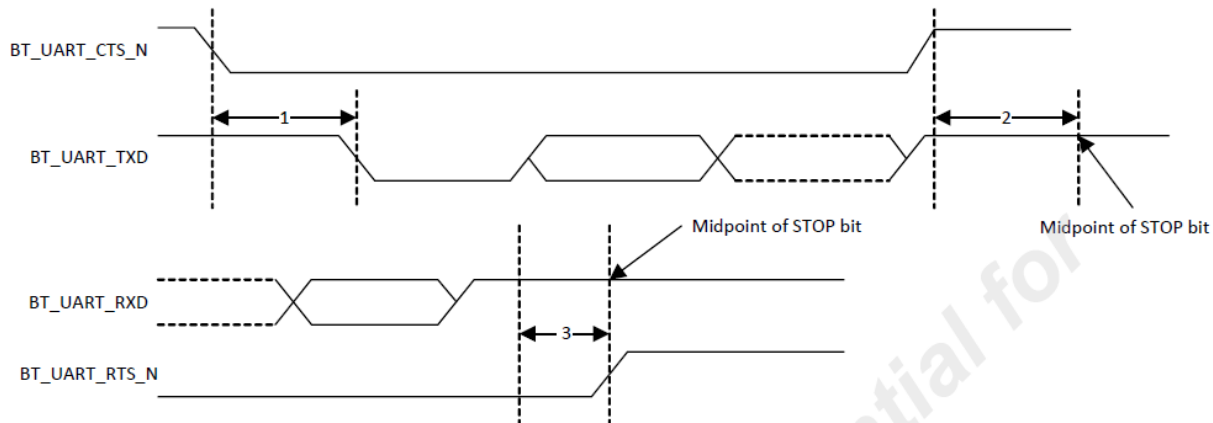


Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns

7.4 UART Interface Description

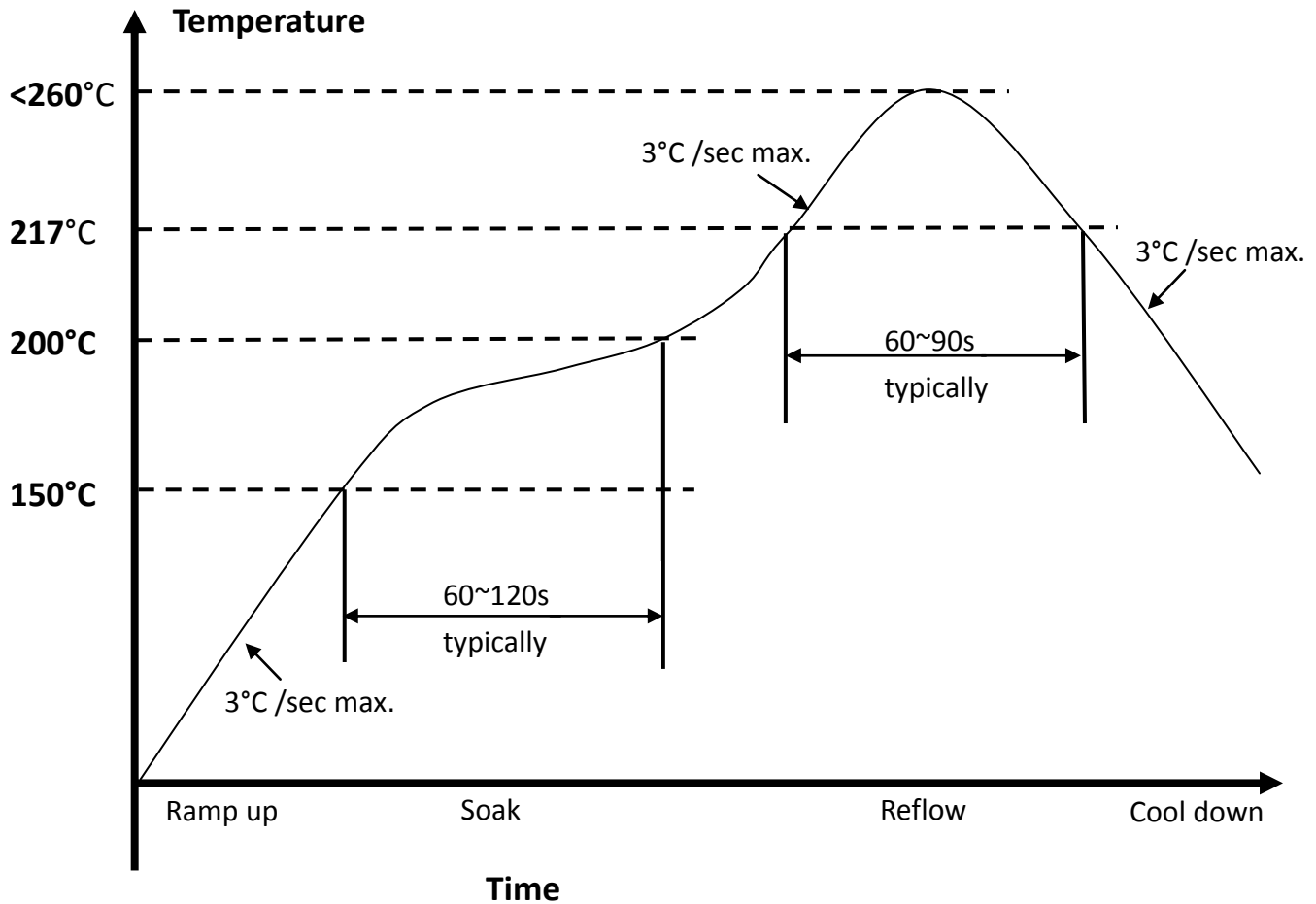
The AP6275SDSR UART is a standard 4-wire interface with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART Timing



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods

8. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C (Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

9. Package Information

9.1 Label

Picture A→ Anti-static and humidity notice



Label B→ MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

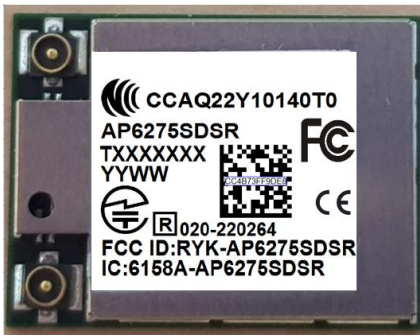
Label C→ Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	 9PKGYMMDDNNNNN
Model Name:	 APXXXXXXXX (R3HF)
P/N:	 99X-XXX-XXXXR
Quantity:	 1000
Date Code:	 YYWW
Lot Code:	 XXXXXXXX
Made in XXXXXX	

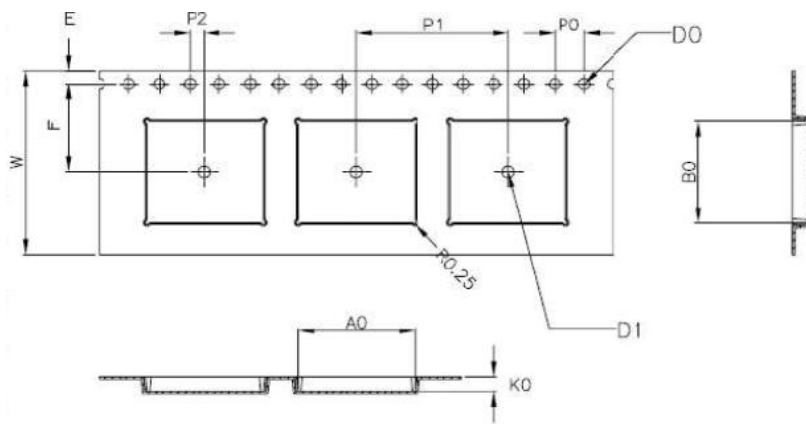
Label D→ Carton box label .

AMPAK Technology Inc.	
PO:	
AMK DEVICE:	
Model Name:	 APXXXXXXXX (R3HF)
Part No.:	 99X-XXX-XXXXR
Quantity:	 5000
Lot D/C:	 XXXXXXXX YYWW 5000
Manufacture:	 YYYY/MM/DD
Made in XXXXXX	

9.2 Dimension

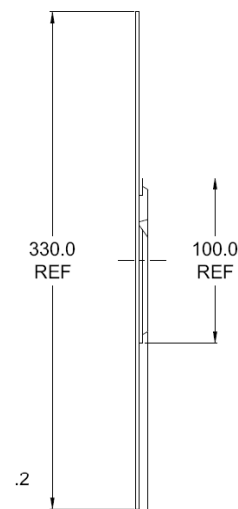
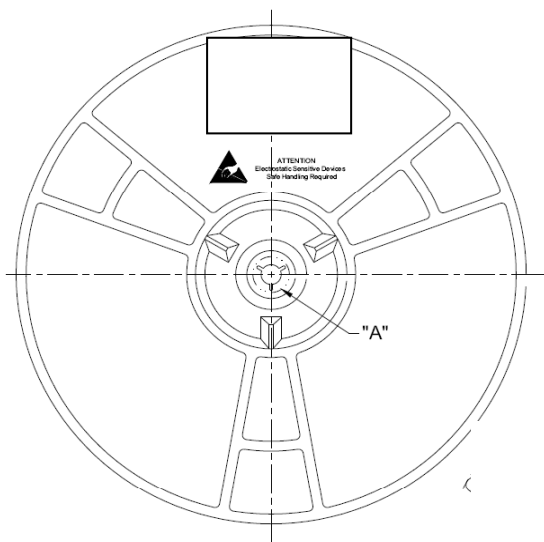


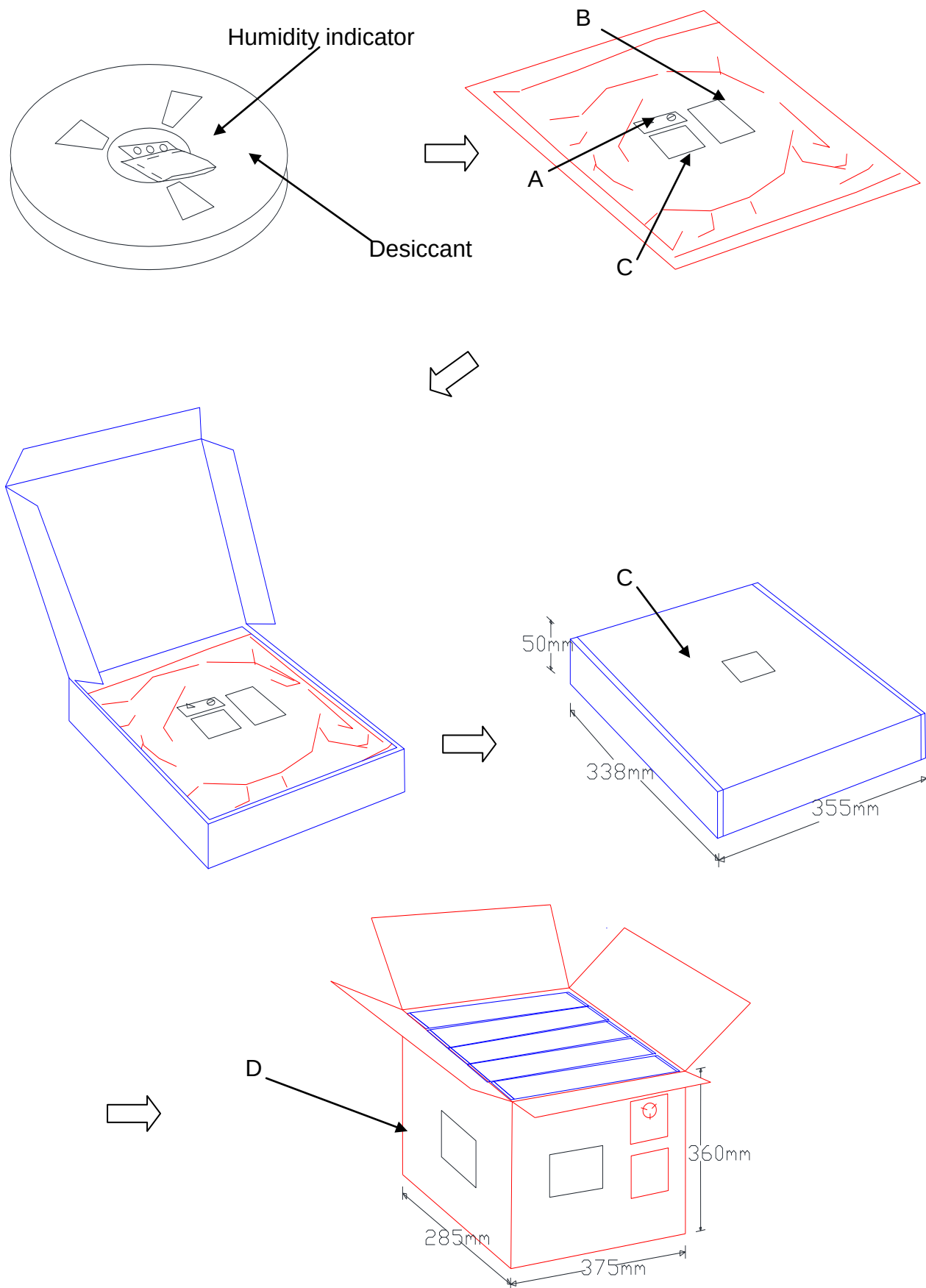
Package	Quantity	Note
Reel/Bag/Box	1000pcs	
Carton	5000pcs	5Box



W	24.00±0.30
A0	15.30±0.10
B0	13.30±0.10
K0	2.00±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	20.00±0.10
P2	2.00±0.10
D0	1.50 $\begin{smallmatrix} +0.10 \\ -0.00 \end{smallmatrix}$
D1	∅1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Component load per 13" reel : 1000 pcs







Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL

4

If blank, see adjacent
bar code label

1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)
2. Peak package body temperature: 250 $^{\circ}\text{C}$
If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 72 hours of factory conditions
If blank, see adjacent bar code label
 $\leq 30^{\circ}\text{C}/60\% \text{ RH}$, or
 - b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
 - a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$
 - b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: _____
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020