



正基科技股份有限公司

SPECIFICATION

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Company	
Representative Signature	

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正基科技股份有限公司



AP6398H

Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2018/04/11	- Draft Spec	Richard
0.2	2018/04/24	- Modify Physical Dimension - Modify Pin assignment	Richard
0.3	2018/07/04	- Modify VBAT Voltage range	Ali
0.4	2018/09/21	- Modify RF Specification	Ali
1.0	2018/09/27	- Release new version datasheet - Modify RF Specification	Ali
1.1	2018/12/21	- Modify 2.4GHz channel list	Richard

Contents

1. Introduction	2
1.1 Overview.....	2
1.2 Product Features.....	3
2. General Specification.....	4
2.1 General Specification.....	4
2.2 DC Characteristics	4
2.2.1 Absolute Maximum Ratings.....	4
2.2.2 Recommended Operating Rating	4
3. Wi-Fi RF Specification	5
3.1 2.4GHz RF Specification	5
4.2 5GHz RF Specification	7
4. Pin Definition	11
4.1 Pin Outline	11
4.2 Pin Definition	11
5. Dimensions.....	14
5.1 Physical Dimensions	14
5.2 Layout Recommendation	15
6. Dimensions.....	16
6.1 Module Dimensions	16
6.2 Recommended footprint.....	16
7. External clock reference	17
8. Host Interface Timing Diagram	18
8.1 Power-up Sequence Timing Diagram.....	18
8.2 SDIO Interface Description	20
8.3 SDIO Default Mode Timing Diagram.....	21
8.4 SDIO High Speed Mode Timing Diagram	22
8.5 SDIO Bus Timing Specifications in SDR Modes	23
8.6 SDIO Bus Timing Specifications in DDR50 Mode	25
9. Recommended Reflow Profile.....	27
10. Package Information	28
10.1 Label	28
10.2 Dimension	29
10.3 MSL Level / Storage Condition	31



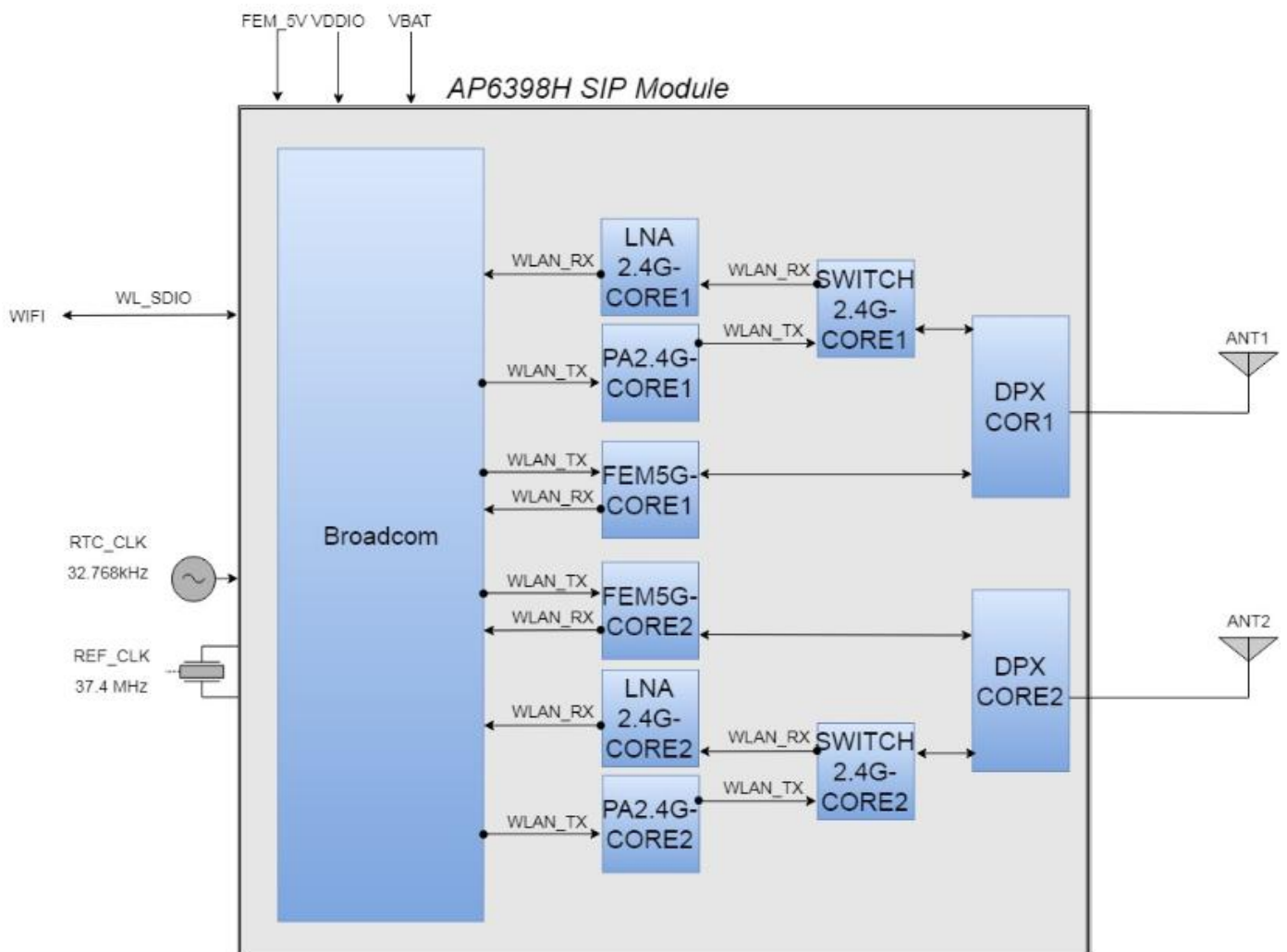
1. Introduction

1.1 Overview

AMPAK Technology would like to announce a low-cost and high-power module which has all of the WiFi functionalities. The highly integrated module makes the possibilities of Drone applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n/ac 2x2 Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 a/b/g/n/ac 2x2 MIMO standard and it can achieve up to a speed of 867Mbps with dual stream in 802.11ac to connect the wireless LAN. The integrated module provides SDIO interface for WiFi.

This compact module is a total solution for a combination of WiFi technologies. The module is specifically developed for drone devices.



1.2 Product Features

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (256 QAM modulation)
- IEEE 802.11 ac/n beam forming.
- Real simultaneous dual-band (RSDB)
- Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP6398H
Product Description	2T2R 802.11 ac/c/b/g/n Wi-Fi + BT 5.0 Module
Dimension	L x W x H: 22 x 21 x 2.2 (typical) mm
WiFi Interface	Support SDIO V3.0/2.0
Operating temperature	-30°C to 65°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.0V < VBAT < 3.6V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
FEM_5V	FEM supply Voltage	0	5.5	V
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.8	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	65	deg.C
FEM_5V	4.5	5	5.25	V
VBAT	3.0	3.3	3.6	V
VDDIO	1.7	1.8,3.3	3.6	V

VBAT current consumption 600mA, when VBAT = 3.3V

FEM_5V current consumption 1000mA(Avg.)/1500mA(Peak), when FEM_5V = 5V



3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11b/g/n & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11 g/n：OFDM /64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	25	25	25	25	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	21	21	20	20	20
	54Mbps				
	20				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	20	20	19	19	19
	MCS7				
	19				
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER ≤ 8%、OFDM modulation PER ≤ 10%					
802.11b	Data Rate	Spec.(dBm)			
	1Mbps	-95			
	2Mbps	-94			
	5.5Mbps	-92			
	11Mbps	-89			
802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)	
	6Mbps	-92	24Mbps	-85	
	9Mbps	-91	36Mbps	-82	
	12Mbps	-90	48Mbps	-77	
	18Mbps	-88	54Mbps	-76	



802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-95	24Mbps	-88
	9Mbps	-94	36Mbps	-85
	12Mbps	-93	48Mbps	-80
	18Mbps	-91	54Mbps	-79
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-82
	MCS1	-89	MCS5	-77
	MCS2	-88	MCS6	-76
	MCS3	-85	MCS7	-74
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-94	MCS5	-80
	MCS1	-92	MCS6	-79
	MCS2	-91	MCS7	-77
	MCS3	-88	MCS8	-89
	MCS4	-85	MCS15	-71
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

4.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz （5GHz UNII Band）			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch140 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	20	20	20	19
	5470~5720	20	20	20	19
	5725~5845	20	20	20	19
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	19	19		
	5470~5720	19	19		
	5725~5845	19	19		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	20	20	19	19
	5470~5720	20	20	19	19
	5725~5845	20	20	19	19
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	19	18		
	5470~5720	19	18		
	5725~5845	19	18		
802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	20	20	18	18
	5470~5720	20	20	18	18
	5725~5845	20	20	18	18
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	18	18		
	5470~5720	18	18		
	5725~5845	18	18		

802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	20	20	19	19
	5470~5720	20	20	19	19
	5725~5845	20	20	19	19
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	19	18	16	
	5470~5720	19	18	16	
	5725~5845	19	18	16	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	20	20	18	18
	5470~5720	20	20	18	18
	5725~5845	20	20	18	18
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	18	18	16	16
	5470~5720	18	18	16	16
	5725~5845	18	18	16	16
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	18	18	18	18
	5470~5720	18	18	18	18
	5725~5845	18	18	18	18
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	18	18	16	15
	5470~5720	18	18	16	15
	5725~5845	18	18	16	15

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$

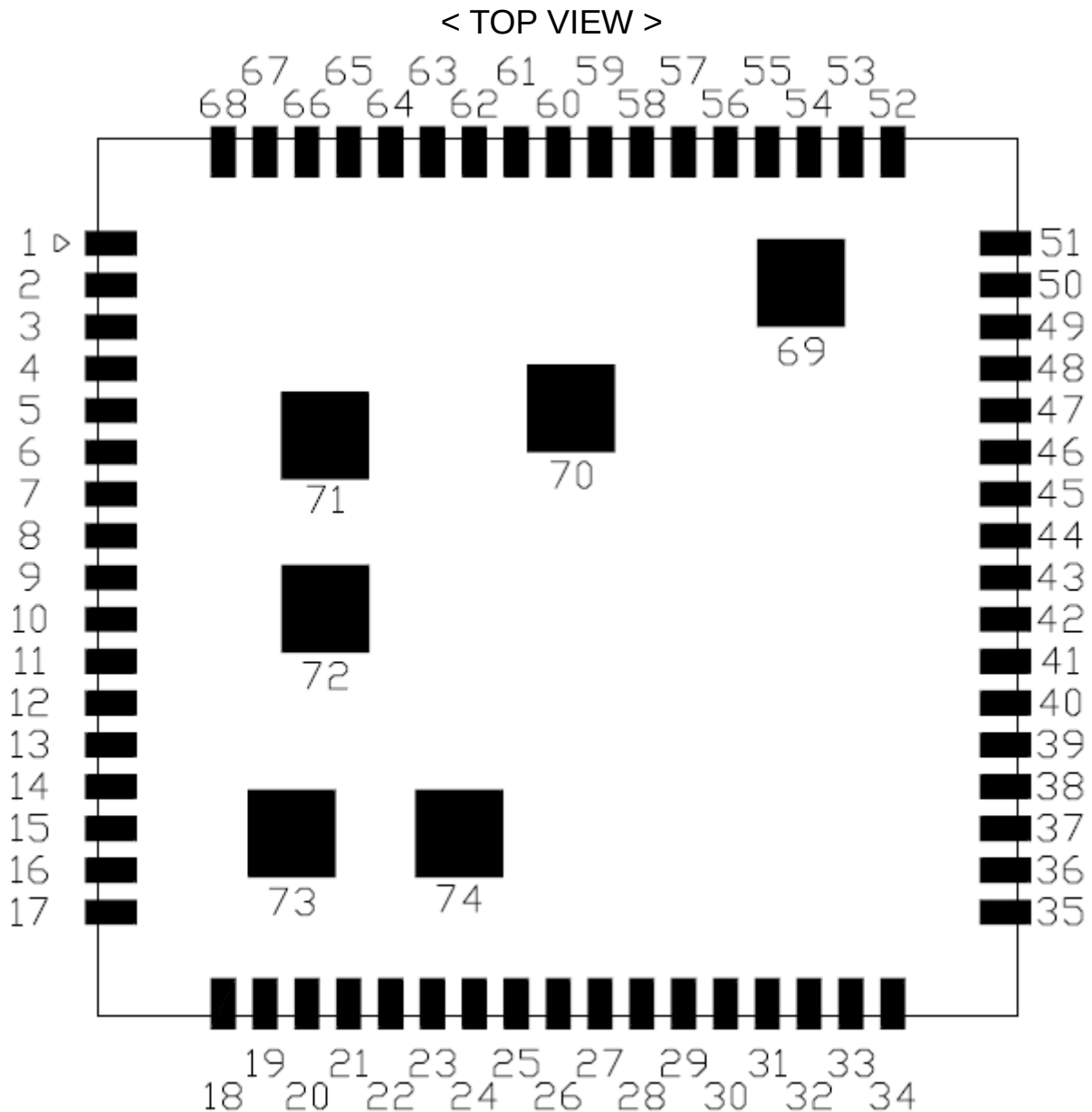
802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-93	24Mbps	-85
	9Mbps	-92	36Mbps	-83
	12Mbps	-91	48Mbps	-78
	18Mbps	-88	54Mbps	-76
802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-96	24Mbps	-88
	9Mbps	-95	36Mbps	-86
	12Mbps	-94	48Mbps	-81
	18Mbps	-91	54Mbps	-79

802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS4	-83
	MCS1	-91	MCS5	-81
	MCS2	-89	MCS6	-76
	MCS3	-86	MCS7	-73.5
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-95	MCS5	-84
	MCS1	-93	MCS6	-79
	MCS2	-92	MCS7	-76.5
	MCS3	-89	MCS8	-90
	MCS4	-86	MCS15	-72
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS4	-78
	MCS1	-87	MCS5	-75
	MCS2	-85	MCS6	-72
	MCS3	-82	MCS7	-71
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
	MCS1	-90	MCS6	-75
	MCS2	-88	MCS7	-74
	MCS3	-85	MCS8	-87
	MCS4	-81	MCS15	-69
802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS5	-81
	MCS1	-90	MCS6	-76
	MCS2	-89	MCS7	-73.5
	MCS3	-86	MCS8	-69
	MCS4	-83		
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-94	MCS6,NSS=1	-78
	MCS1,NSS=1	-93	MCS7,NSS=1	-77
	MCS2,NSS=1	-72	MCS8,NSS=1	-71
	MCS3,NSS=1	-89	MCS0,NSS=2	-90
	MCS4,NSS=1	-86	MCS8,NSS=2	-66
	MCS5,NSS=1	-81		

802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS5	-75
	MCS1	-87	MCS6	-72
	MCS2	-85	MCS7	-71
	MCS3	-82	MCS8	-67
	MCS4	-78	MCS9	-65
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-91	MCS6,NSS=1	-74
	MCS1,NSS=1	-89	MCS7,NSS=1	-73
	MCS2,NSS=1	-87	MCS8,NSS=1	-68
	MCS3,NSS=1	-84	MCS9,NSS=1	-66
	MCS4,NSS=1	-80	MCS0,NSS=2	-88
	MCS5,NSS=1	-77	MCS9,NSS=2	-63
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS5	-72
	MCS1	-84	MCS6	-70
	MCS2	-82	MCS7	-66
	MCS3	-78	MCS8	-64
	MCS4	-75	MCS9	-61
802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-89	MCS6,NSS=1	-72
	MCS1,NSS=1	-86	MCS7,NSS=1	-68
	MCS2,NSS=1	-84	MCS8,NSS=1	-66
	MCS3,NSS=1	-80	MCS9,NSS=1	-63
	MCS4,NSS=1	-77	MCS0,NSS=2	-87
	MCS5,NSS=1	-74	MCS9,NSS=2	-61
Maximum Input Level	802.11a/n/ac : -30 dBm			

4. Pin Definition

4.1 Pin Outline



4.2 Pin Definition

NO	Name	Type	Description
1	GND	P	Ground connections
2	WL_ANT0	RF	RF Port 0
3	GND	P	Ground connections
4	GND	P	Ground connections
5	GND	P	Ground connections
6	GND	P	Ground connections
7	GND	P	Ground connections



8	GND	P	Ground connections
9	GND	P	Ground connections
10	GND	P	Ground connections
11	GND	P	Ground connections
12	GND	P	Ground connections
13	GND	P	Ground connections
14	WL_ANT1	RF	RF Port 1
15	GND	P	Ground connections
16	GND	P	Ground connections
17	GND	P	Ground connections
18	NC	—	Floating (Do not connect to GND)
19	GND	P	Ground connections
20	XTAL_OUT	I/O	External Crystal out
21	XTAL_IN	I/O	External Crystal in/ Single clock source in
22	GND	P	Ground connections
23	NC	—	Floating (Do not connect to GND)
24	NC	—	Floating (Do not connect to GND)
25	GND	P	Ground connections
26	SDIO_DATA_2	I/O	SDIO data line 2
27	SDIO_DATA_3	I/O	SDIO data line 3
28	SDIO_DATA_CMD	I/O	SDIO command line
29	SDIO_DATA_CLK	I/O	SDIO clock line
30	SDIO_DATA_0	I/O	SDIO data line 0
31	SDIO_DATA_1	I/O	SDIO data line 1
32	GND	P	Ground connections
33	WL_UART_RX	I/O	WL UART DATA RX(debug).
34	WL_UART_TX	I/O	WL UART DATA TX(debug).
35	NC	—	Floating (Do not connect to GND)
36	NC	—	Floating (Do not connect to GND)
37	NC	—	Floating (Do not connect to GND)
38	NC	—	Floating (Do not connect to GND)
39	GND	P	Ground connections
40	VDDIO	P	I/O Voltage supply input
41	GND	P	Ground connections
42	LPO	I	External Low Power Clock input (32.768KHz)
43	GND	P	Ground connections
44	VBAT	P	Main power voltage source input

45	GND	P	Ground connections
46	SDIO_VSEL	I	SDIO Voltage level selection 1: 1.8V(default) 、 0: 3.3V
47	GND	P	Ground connections
48	FEM_5V	P	FEM voltage source input
49	FEM_5V	P	FEM voltage source input
50	GND	P	Ground connections
51	VIN_LDO_OUT	P	Internal Buck voltage generation pin
52	VIN_LDO	P	Internal Buck voltage supply pin
53	GND	P	Ground connections
54	NC	—	Floating (Do not connect to GND)
55	WL_REG_ON	I	Low asserting reset for WiFi core
56	GND	P	Ground connections
57	NC	—	Floating (Do not connect to GND)
58	GND	P	Ground connections
59	NC	—	Floating (Do not connect to GND)
60	NC	—	Floating (Do not connect to GND)
61	NC	—	Floating (Do not connect to GND)
62	NC	—	Floating (Do not connect to GND)
63	GND	P	Ground connections
64	WL_HOST_WAKE	O	WLAN to wake-up HOST
65	NC	—	Floating (Do not connect to GND)
66	NC	—	Floating (Do not connect to GND)
67	NC	—	Floating (Do not connect to GND)
68	GND	P	Ground connections
69	GND	P	Ground connections
70	GND	P	Ground connections
71	GND	P	Ground connections
72	GND	P	Ground connections
73	GND	P	Ground connections
74	GND	P	Ground connections

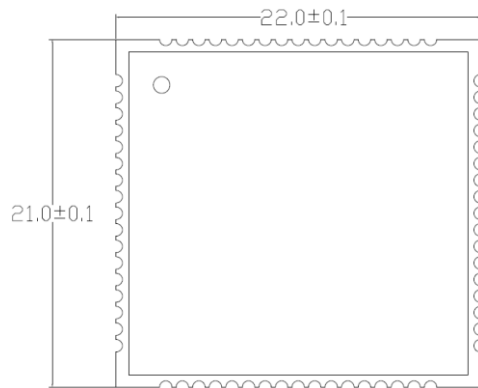


5. Dimensions

5.1 Physical Dimensions

(Unit: mm)

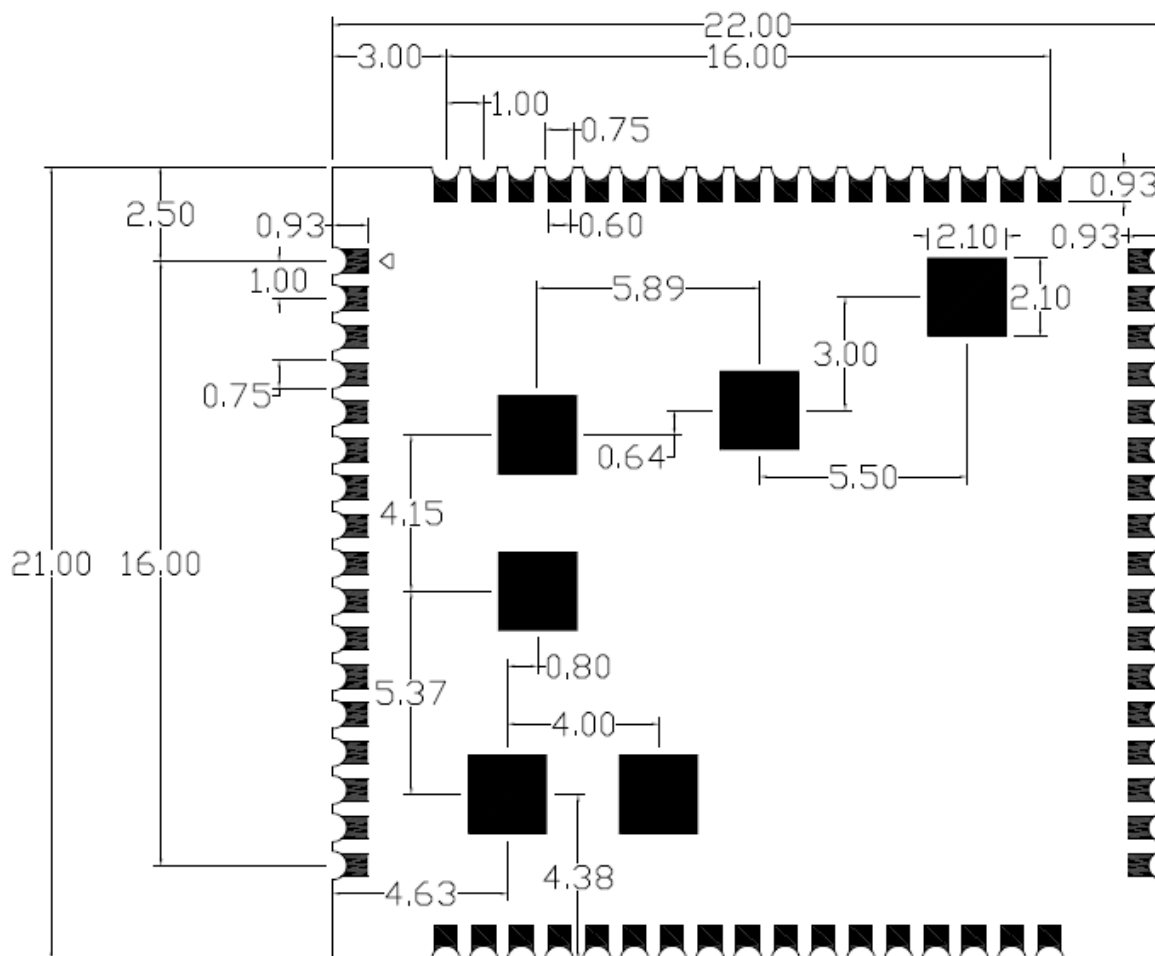
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< Side View >



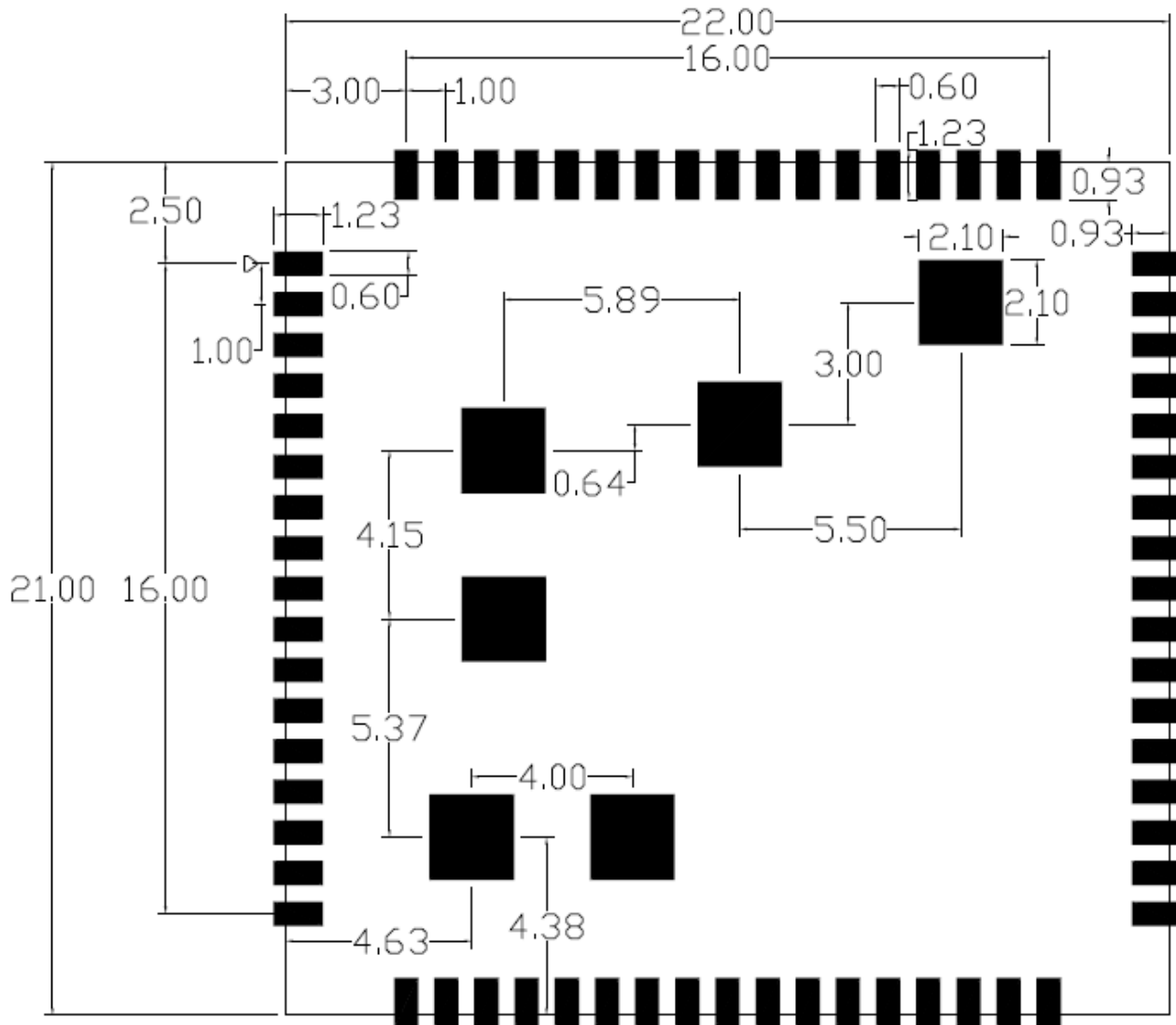
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5.2 Layout Recommendation

(Unit: mm)

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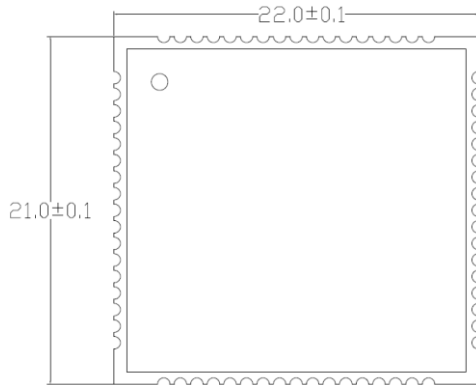


6. Dimensions

6.1 Module Dimensions

(Unit: mm)

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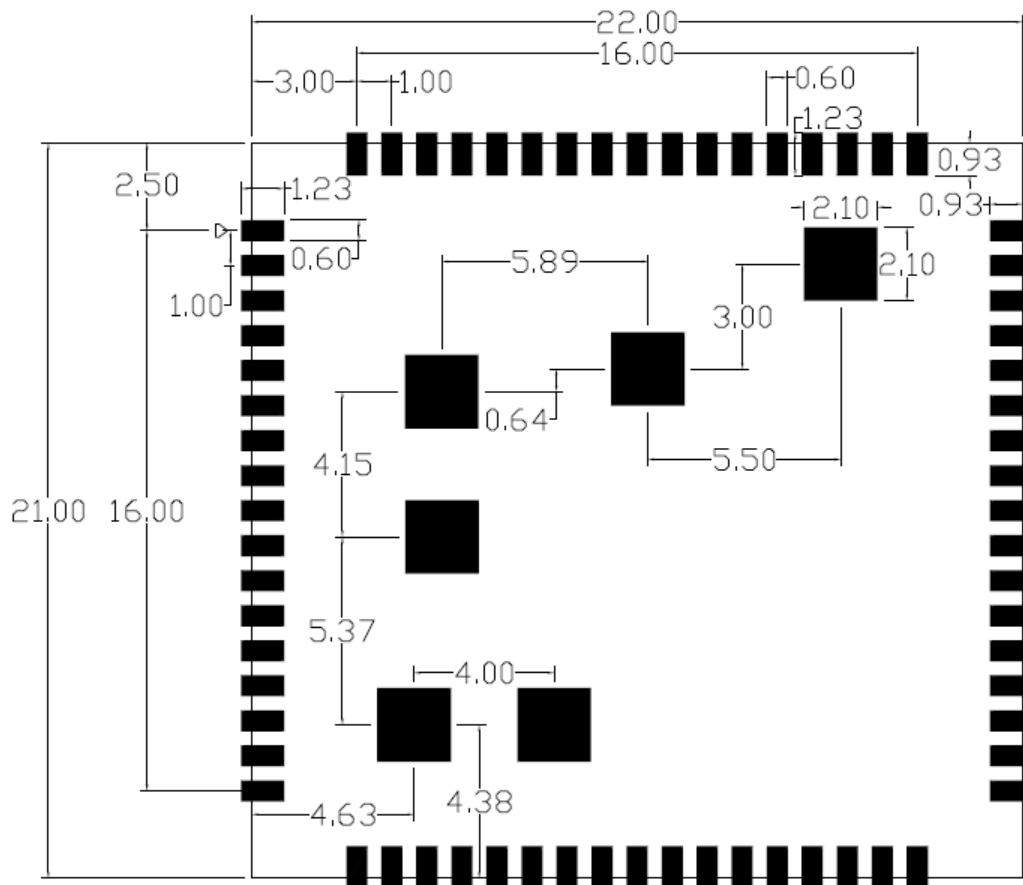


< Side View >



< TOP VIEW >

6.2 Recommended footprint

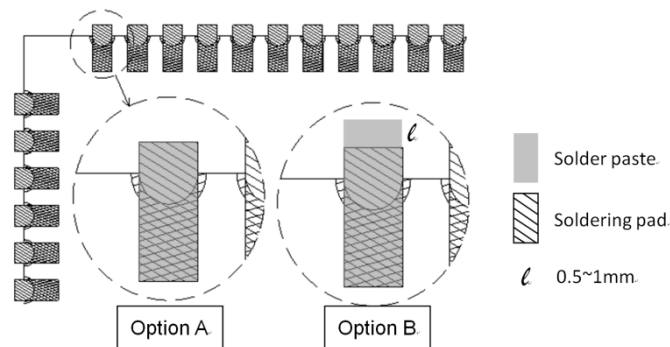


- Solder paste layer design is generally the same as recommended footprint.



(錫膏層設計通常建議和焊墊尺寸相同)

- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial. In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊)。



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

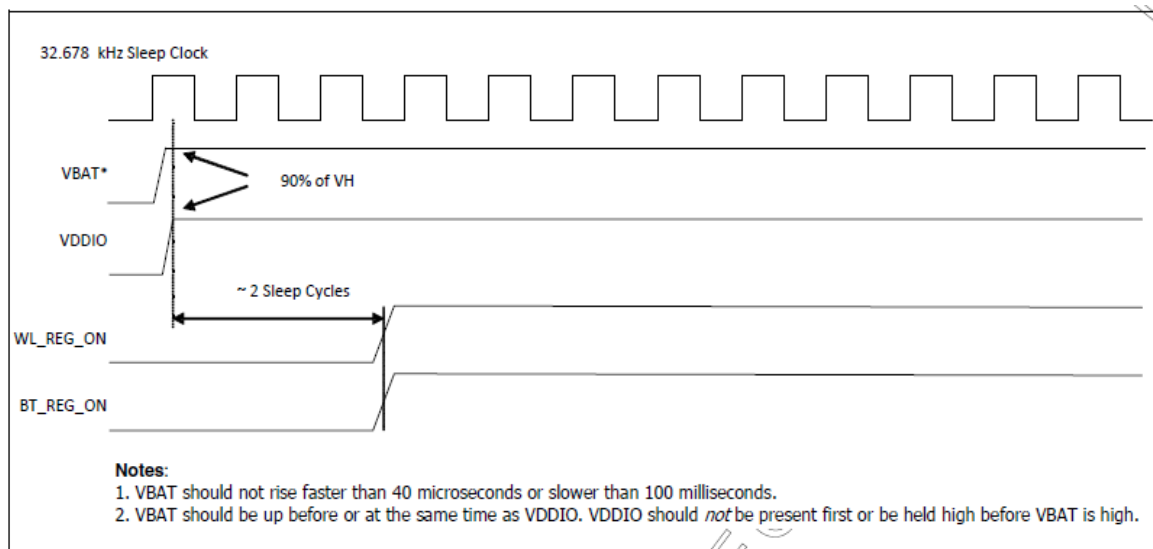
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

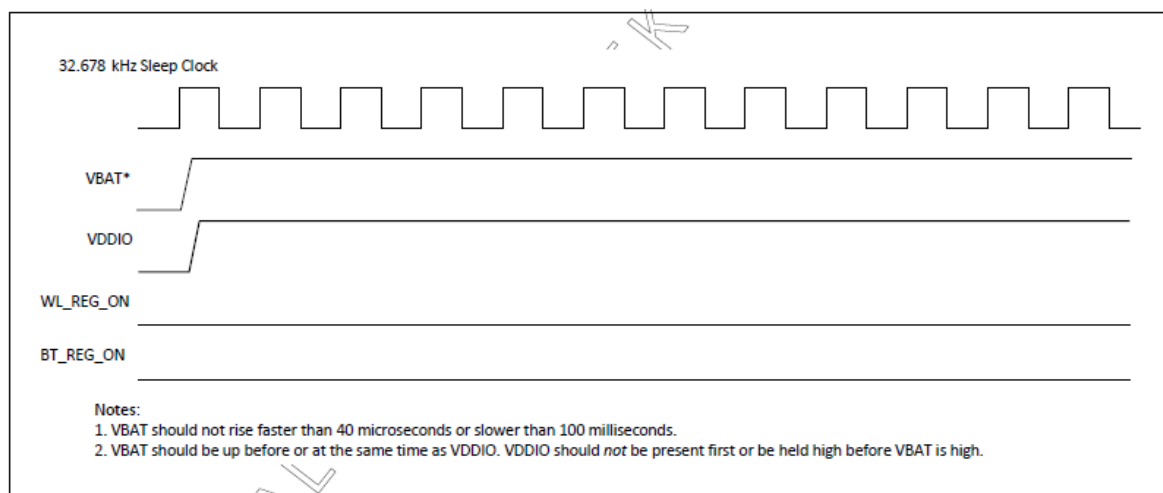
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

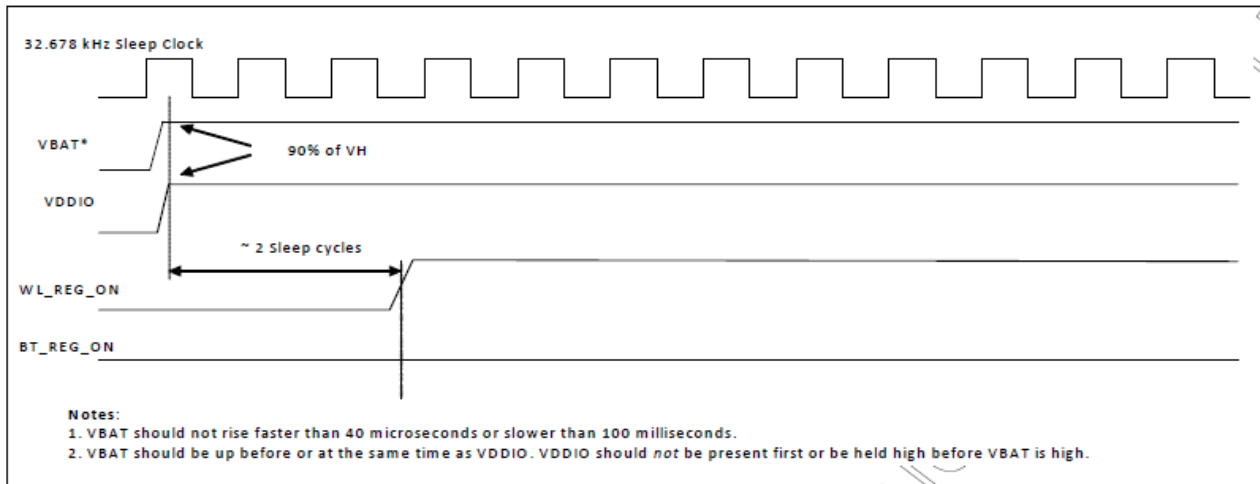
- **WL_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



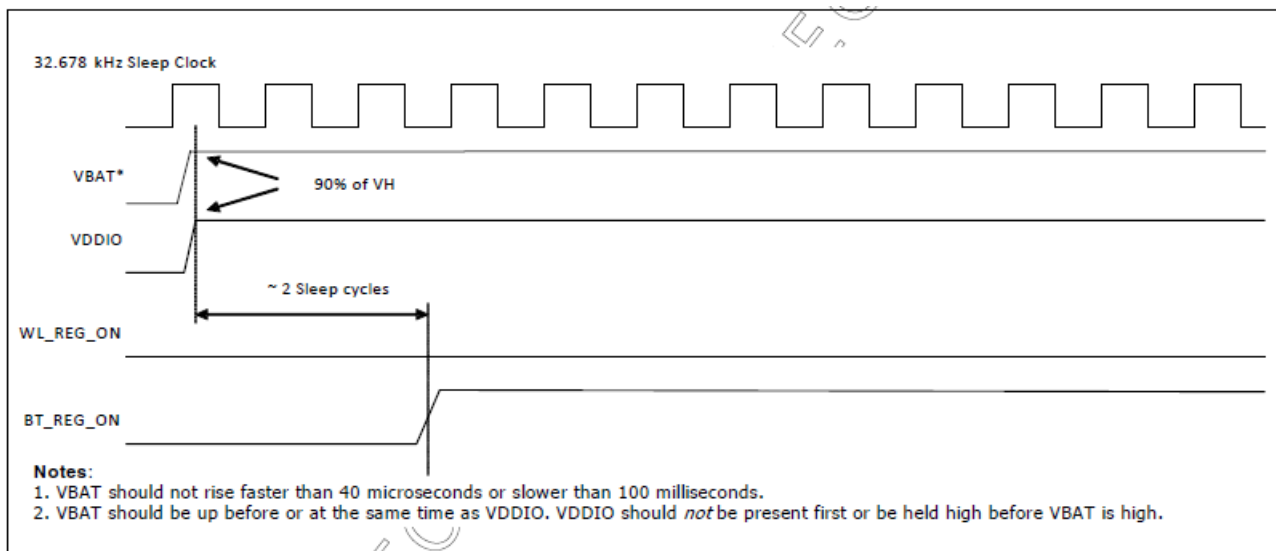
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

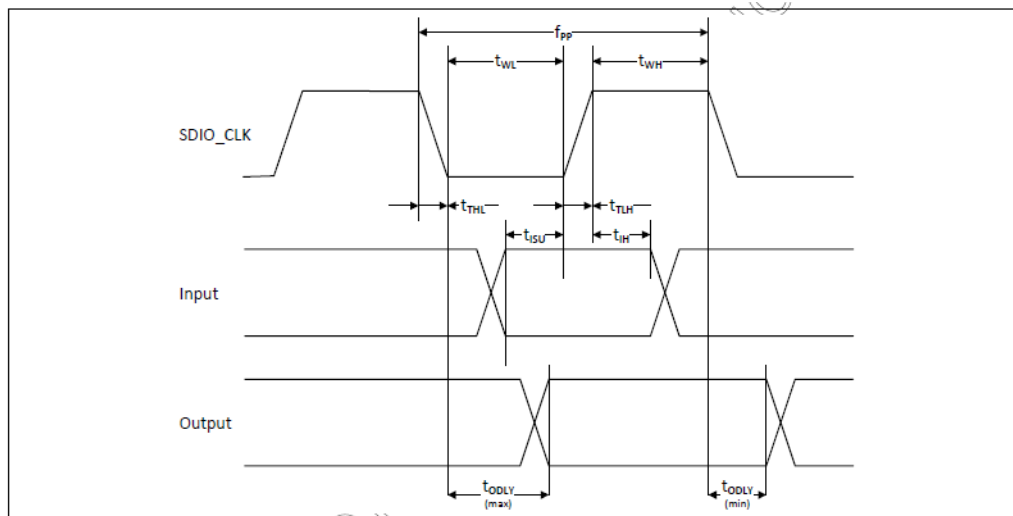
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

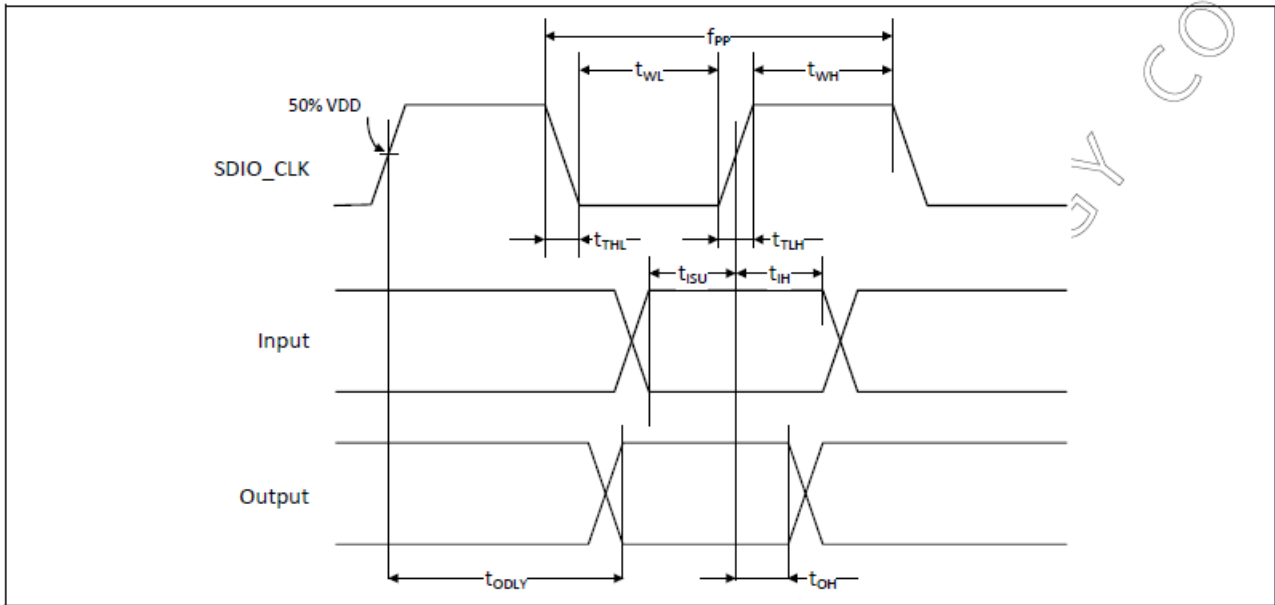
8.3 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

- a. Timing is based on $CL \leq 40pF$ load on CMD and Data.
 b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

8.4 SDIO High Speed Mode Timing Diagram



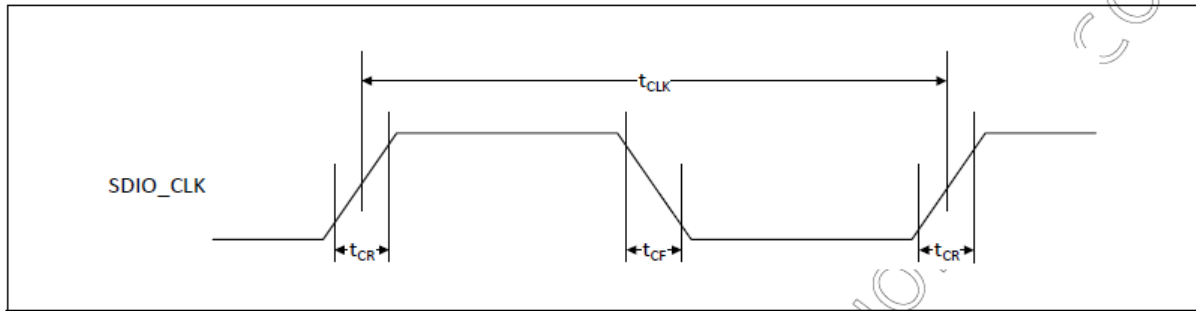
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f_{PP}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on $CL \leq 40$ pF load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

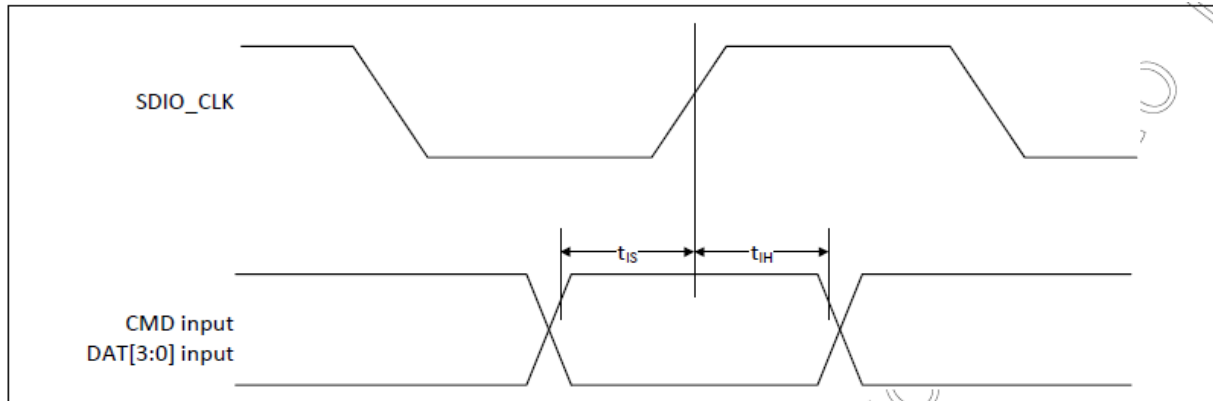
8.5 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	–	30	70	%	–

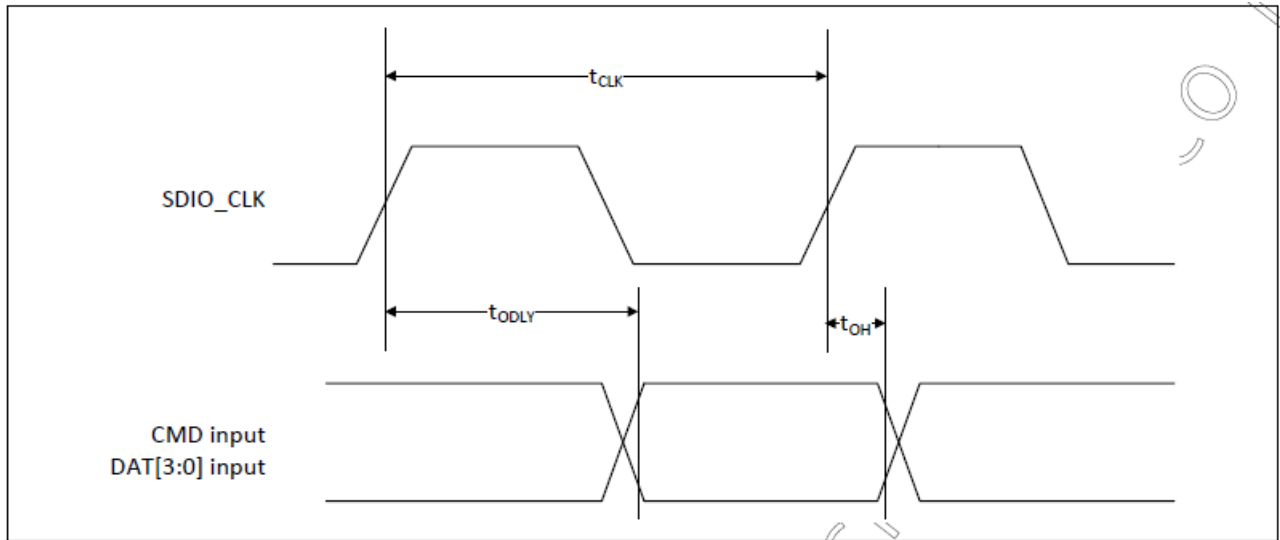
SDIO Bus Input timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

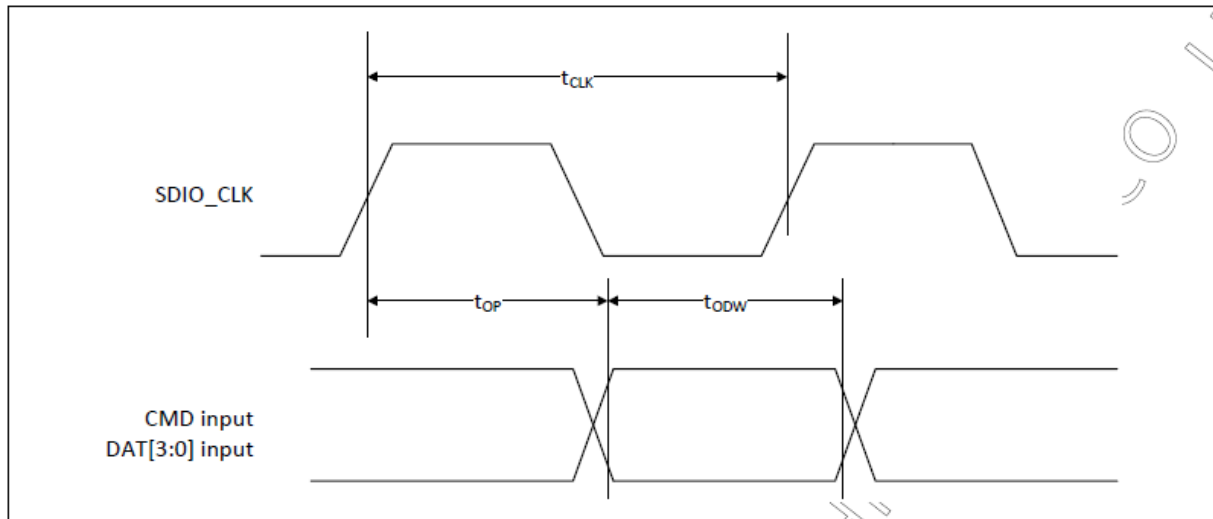


SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

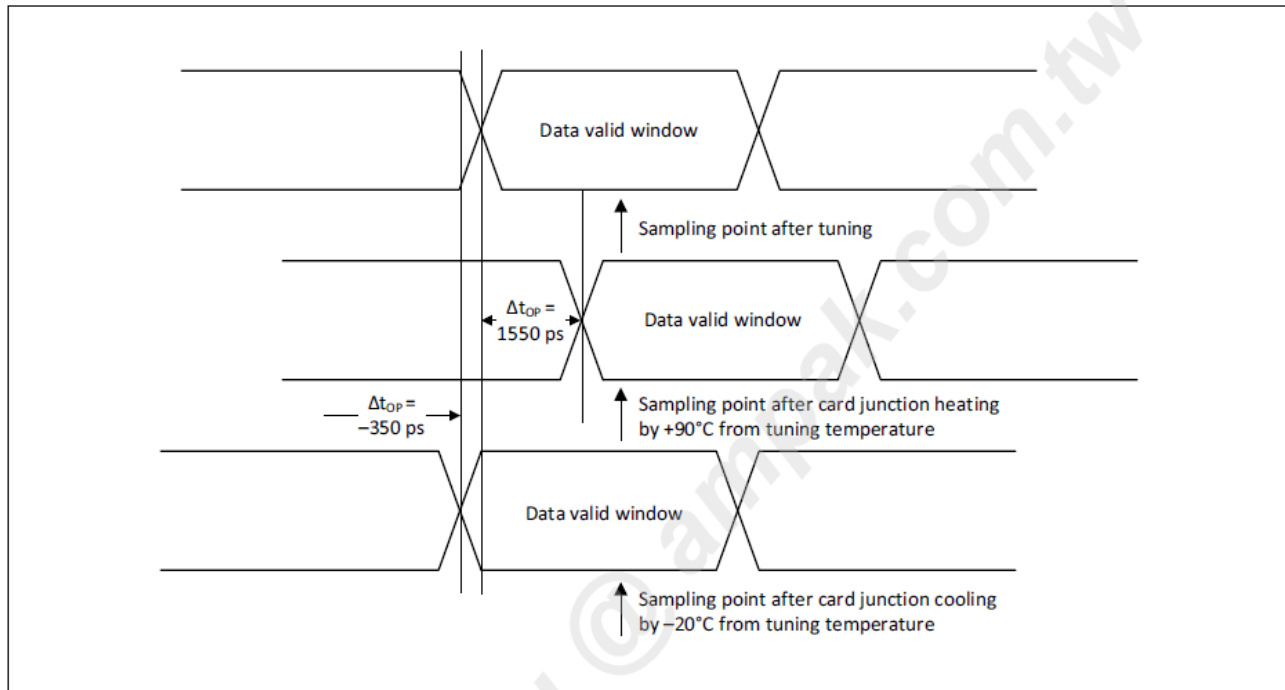
Card output timing (SDR Modes 100MHz to 208MHz)



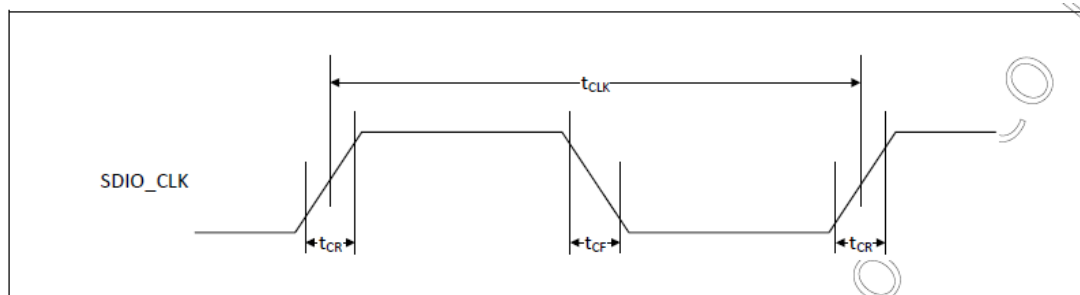
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	$t_{ODW} = 2.88$ ns @ 208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

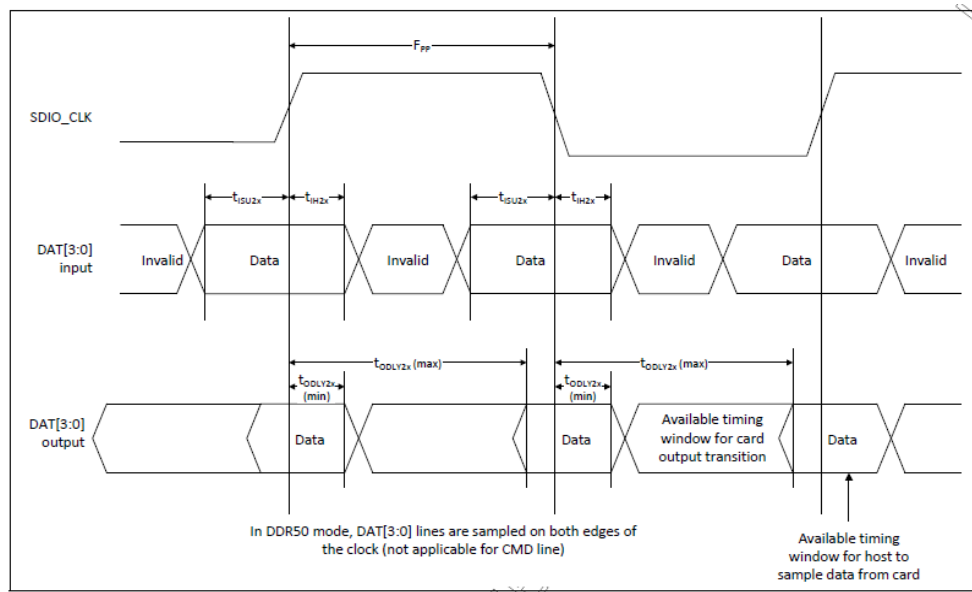


8.6 SDIO Bus Timing Specifications in DDR50 Mode



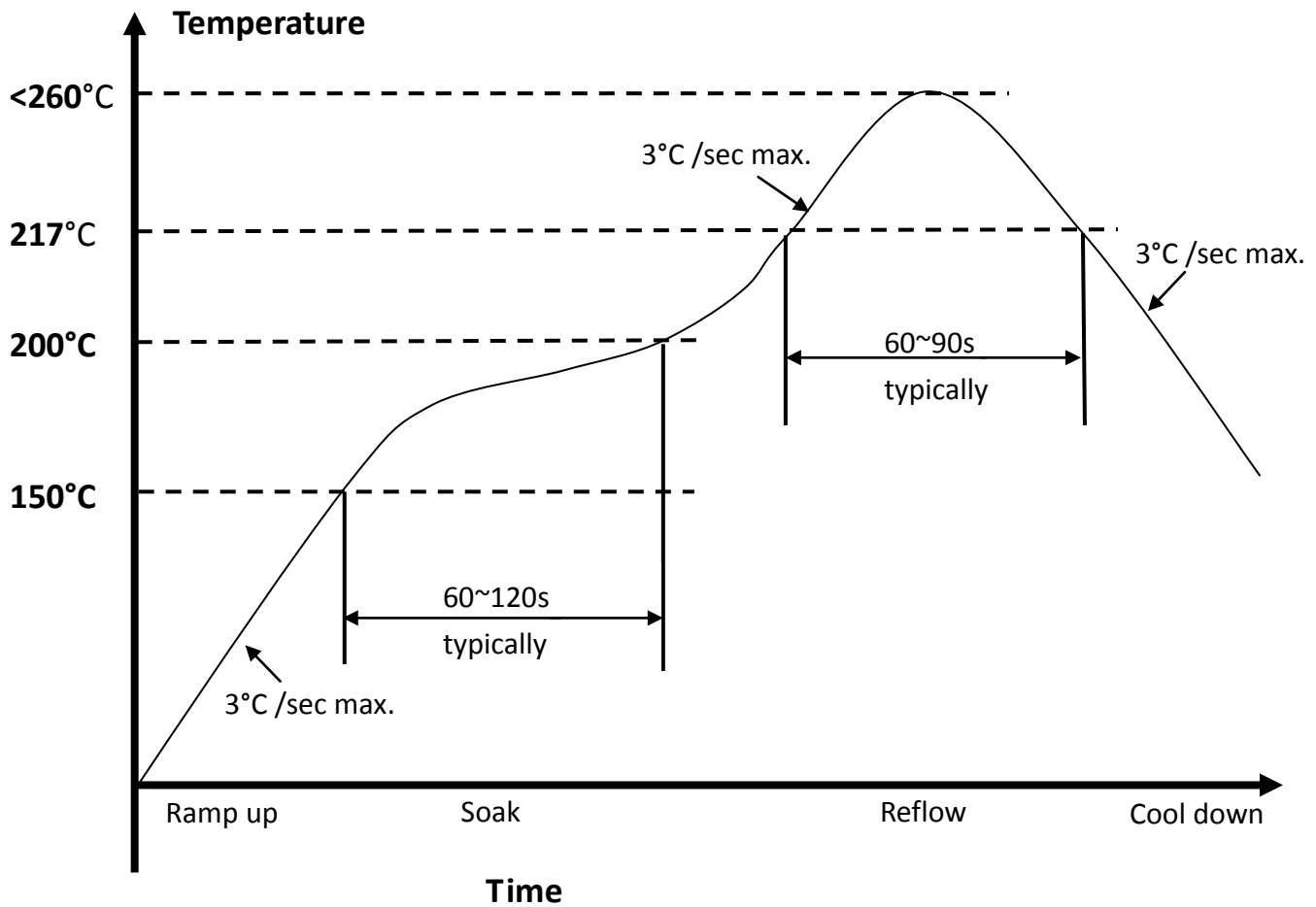
Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00 \text{ ns (max) @ 50 MHz, } C_{CARD} = 10 \text{ pF}$
Clock duty	—	45	55	%	—

Data Timing



Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30 \text{ pF}$ (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10 \text{ pF}$ (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25 \text{ pF}$ (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15 \text{ pF}$ (1 Card)

9. Recommended Reflow Profile

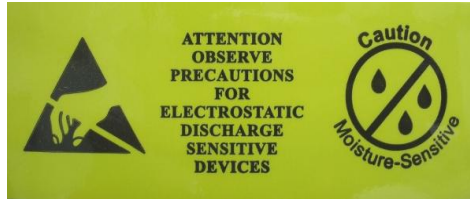


1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

10.1 Label

Label A → Anti-static and humidity notice



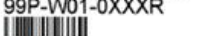
Label B → MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		☐
		If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C # blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions # blank, see adjacent bar code label b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ # blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

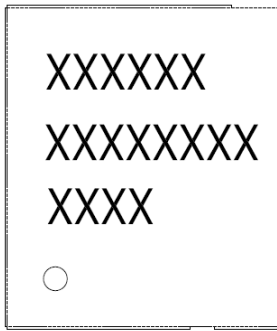
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	
Model :	
P/N:	
Qty :	
Date Code :	
Lot Code :	

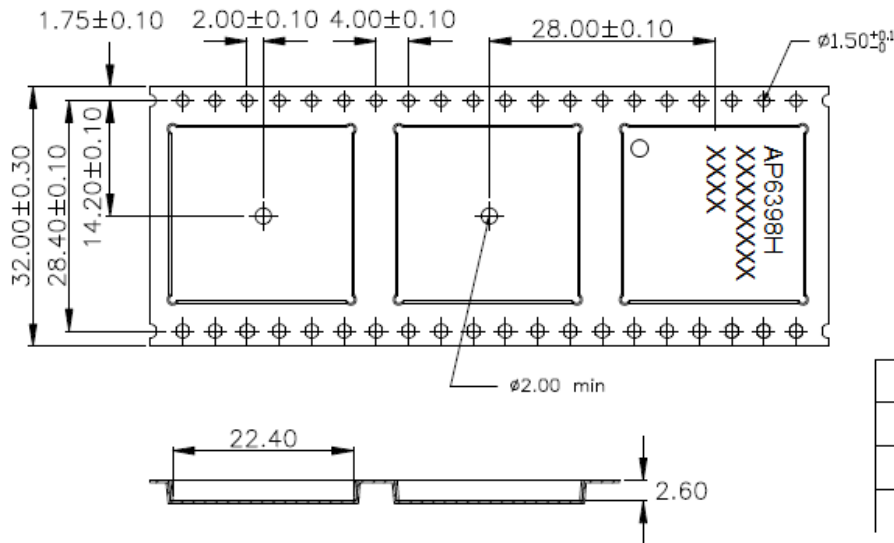
Label D → Carton box label .

AMPAK Technology	
PO :	
AMK DEVICE:	
Model Name :	
Part No.:	
Quantity :	
Lot D/C:	
Manufacture:	

10.2 Dimension

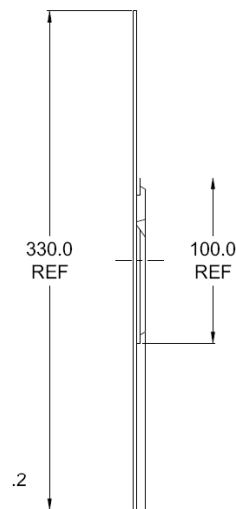
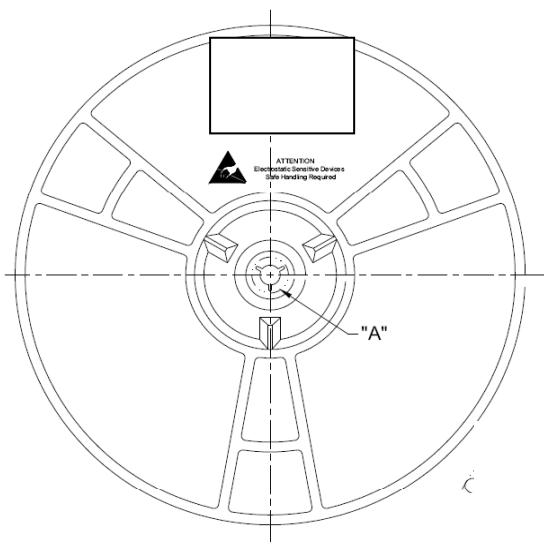


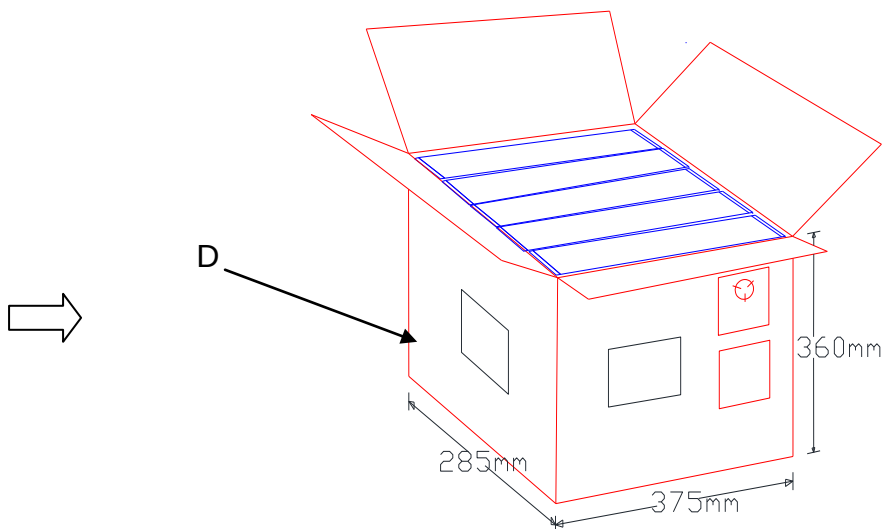
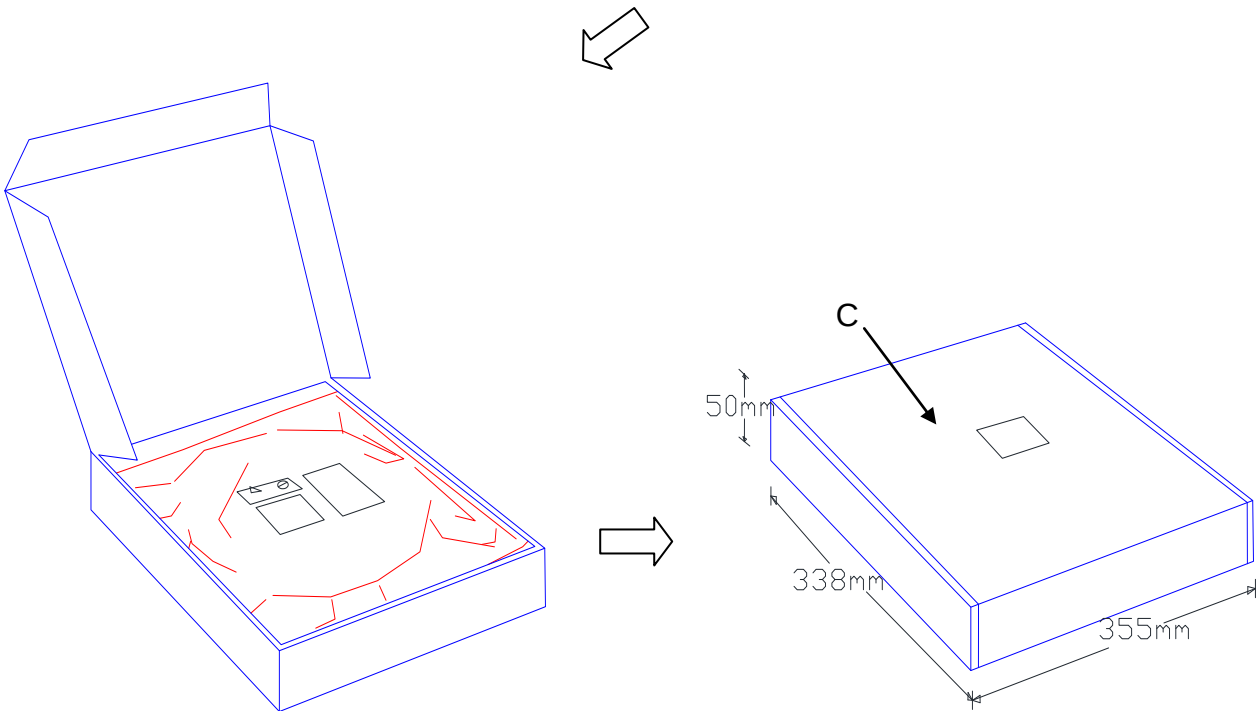
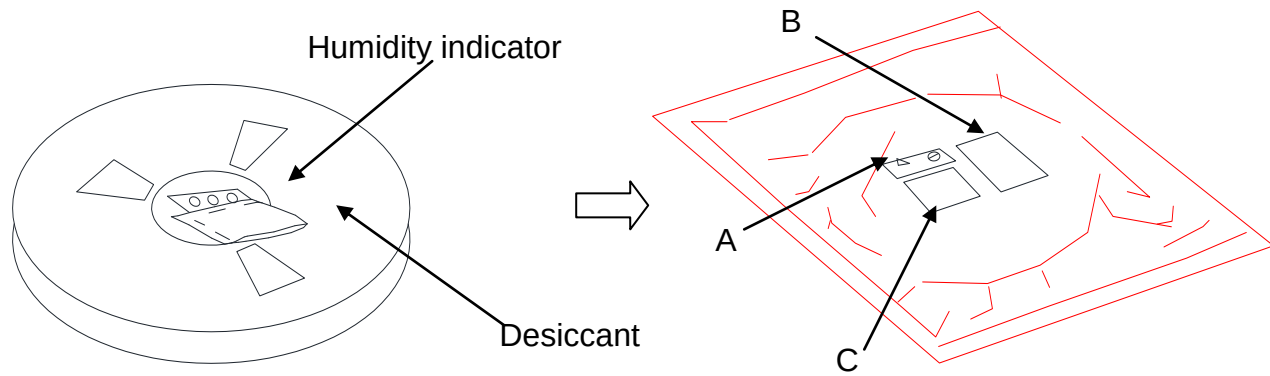
— Part Number
— Lot Code
— Date Code



W	32.00±0.30
A0	22.40±0.10
B0	21.40±0.10
K0	2.60±0.10

1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 60.0 Meters.(1:3)
7. Component load per 13" reel : 500 pcs.





10.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 4 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)		
2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label		
$\leq 30^{\circ}\text{C} / 60\% \text{ RH}$, or		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$		
b) 3a or 3b are not met.		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.		
Bag Seal Date: _____ If blank, see adjacent bar code label		
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		