

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP6398P2

REVISION : 1.1

DATE : Jun. 25th , 2021

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		



正基科技股份有限公司



AP6398P2 Data Sheet

Address:

8F., No.15-1, Zhonghua Rd., Hukou Township, Hsinchu County, Taiwan,
30352

Website:

<http://www.ampak.com.tw>



Revision

Revision	Date	Description	Revised By
1.0	2021/02/08	- Official release	Richard
1.1	2021/06/25	- Official release	Richard

Contents

1. Introduction	2
1.1 Overview	2
1.2 Product Features	3
2. General Specification	4
2.1 General Specification	4
2.2 DC Characteristics	4
2.2.1 Absolute Maximum Ratings	4
2.2.2 Recommended Operating Rating	5
3. Wi-Fi RF Specification	6
3.1 2.4GHz RF Specification	6
3.2 5GHz RF Specification	8
4. Bluetooth Specification	13
4.1 Bluetooth Specification	13
5. Pin Definition	14
5.1 Pin Outline	14
5.2 Pin Assignment	14
6. Dimensions	16
6.1 Module Dimensions	16
6.2 Recommended footprint	17
7. External clock reference	18
8. Host Interface Timing Diagram	19
8.1 Power-up Sequence Timing Diagram	19
8.2 PCIe Interface Description	21
8.3 PCM Interface Description	24
8.4 UART Interface Description	28
9. Recommended Reflow Profile	29
10. Package Information	30
10.1 Label	30
10.2 Dimension	31
10.3 MSL Level / Storage Condition	33

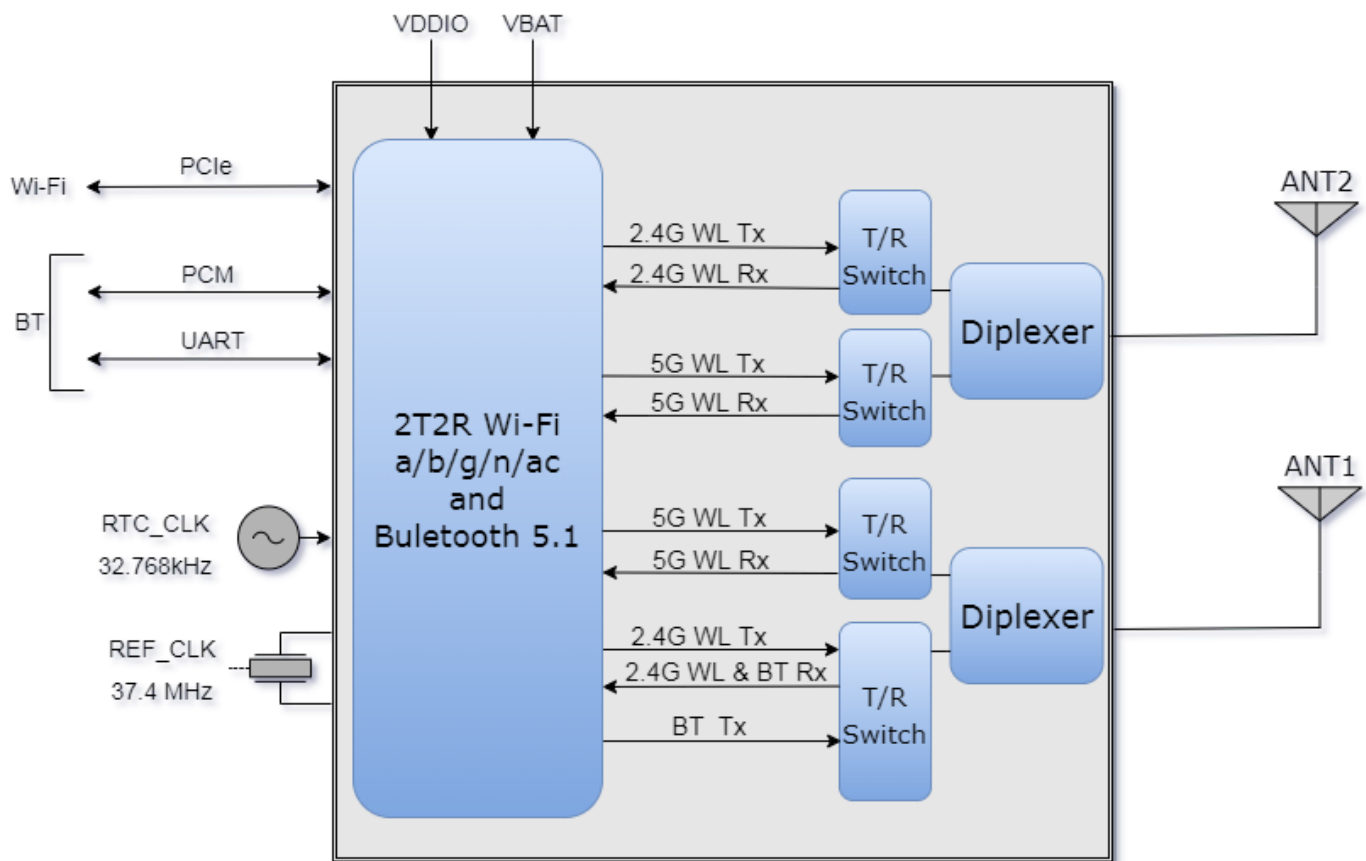


1. Introduction

1.1 Overview

The AMPAK Technology® AP6398P2 is a fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac 2x2 Access Points with MIMO standard and can accomplish up to speed of 867Mbps with dual stream in 802.11ac to connect the wireless LAN. Furthermore AP6398P2 included PCIe interface for Wi-Fi, UART/PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 867 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI. (867 QAM modulation)
- IEEE 802.11ac beam forming.
- Supports 2 antennas with one for shared BT and WLAN port.
 - Supports PCI express revision 3.0 and power management running at Gen1 speeds.
- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.1 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP6398P2
Product Description	2T2R 802.11 ac/a/b/g/n Wi-Fi + BT 5.1 Module
Dimension	L x W: 15 x 13(typical) mm H: 1.60(Maximum) mm
WiFi Interface	Support PCIe v3.0 compliant and runs at Gen1 speeds.
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and $3.2V < V_{BAT} < 3.8V$ without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/ Bluetooth/ I/O Voltage	-0.5	2.07	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 2000mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
VIH	$0.65 \times VDDIO$	N/A	V
VIL	N/A	$0.4 \times VDDIO$	V
VOH output@2mA	$VDDIO - 0.4$	N/A	V
VOL output@2mA	N/A	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11b/g/n & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DBPSK、DQPSK、CCK 802.11 g/n：OFDM /64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19.5	19.5	19.5	19.5	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	19	19	18.5	18.5	18
	54Mbps				
	18				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	19	18.5	18.5	18	18
	MCS7				
	17				
Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB					
CCK modulation PER ≤ 8%、OFDM modulation PER ≤ 10%					
802.11b	Data Rate	Spec.(dBm)			
	1Mbps	-97			
	2Mbps	-93			
	5.5Mbps	-91			
	11Mbps	-89			



802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-93	24Mbps	-85
	9Mbps	-92	36Mbps	-82
	12Mbps	-91	48Mbps	-78
	18Mbps	-88	54Mbps	-76
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-95	24Mbps	-87
	9Mbps	-94	36Mbps	-84
	12Mbps	-93	48Mbps	-81
	18Mbps	-90	54Mbps	-78
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS4	-81.5
	MCS1	-89	MCS5	-79
	MCS2	-87	MCS6	-76
	MCS3	-84	MCS7	-75
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-93	MCS5	-80
	MCS1	-92	MCS6	-78
	MCS2	-90	MCS7	-76
	MCS3	-87	MCS8	-72
	MCS4	-83	MCS15	-73
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz (5GHz UNII Band)			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch144 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	16.5	16.5	16	16
	5470~5720	16.5	16.5	16	16
	5725~5845	16.5	16.5	16	16
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	15.5	15.5		
	5470~5720	15.5	15.5		
	5725~5845	15.5	15.5		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	14.5	14.5		
	5470~5720	14.5	14.5		
	5725~5845	14.5	14.5		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15	15
	5470~5720	16	16	15	15
	5725~5845	16	16	15	15
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	14.5	14.5		
	5470~5720	14.5	14.5		
	5725~5845	14.5	14.5		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	16	15.5	15.5
	5470~5720	16	16	15.5	15.5
	5725~5845	16	16	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	14.5	14.5	12	
	5470~5720	14.5	14.5	12	
	5725~5845	14.5	14.5	12	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	15	15	15
	5470~5720	16	15	15	15
	5725~5845	16	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14.5	14.5	12	10
	5470~5720	14.5	14.5	12	10
	5725~5845	14.5	14.5	12	10
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16	15	14.5	14.5
	5470~5720	16	15	14.5	14.5
	5725~5845	16	15	14.5	14.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	14	14	10	10
	5470~5720	14	14	10	10
	5725~5845	14	14	10	10

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB				
OFDM modulation PER $\leq 10\%$				
802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-89	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
MIMO802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-86
	9Mbps	-91	36Mbps	-83
	12Mbps	-90	48Mbps	-78
	18Mbps	-89	54Mbps	-77
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-76
	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-71
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
	MCS1	-91	MCS6	-76
	MCS2	-89	MCS7	-74
	MCS3	-86	MCS8	-89
	MCS4	-82	MCS15	-70
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-68
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-71
	MCS3	-83	MCS8	-86
	MCS4	-79	MCS15	-67

802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-92	MCS6,NSS=1	-76
	MCS1,NSS=1	-91	MCS7,NSS=1	-75
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-85	MCS0,NSS=2	-88
	MCS4,NSS=1	-82	MCS8,NSS=2	-65
	MCS5,NSS=1	-77		
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-90	MCS6,NSS=1	-73
	MCS1,NSS=1	-88	MCS7,NSS=1	-72
	MCS2,NSS=1	-86	MCS8,NSS=1	-68
	MCS3,NSS=1	-82	MCS9,NSS=1	-66
	MCS4,NSS=1	-79	MCS0,NSS=2	-86
	MCS5,NSS=1	-77	MCS9,NSS=2	-60
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-87	MCS6,NSS=1	-70
	MCS1,NSS=1	-85	MCS7,NSS=1	-68
	MCS2,NSS=1	-82	MCS8,NSS=1	-66
	MCS3,NSS=1	-79	MCS9,NSS=1	-63
	MCS4,NSS=1	-76	MCS0,NSS=2	-83
	MCS5,NSS=1	-71	MCS9,NSS=2	-58
Maximum Input Level	802.11a/n/ac : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

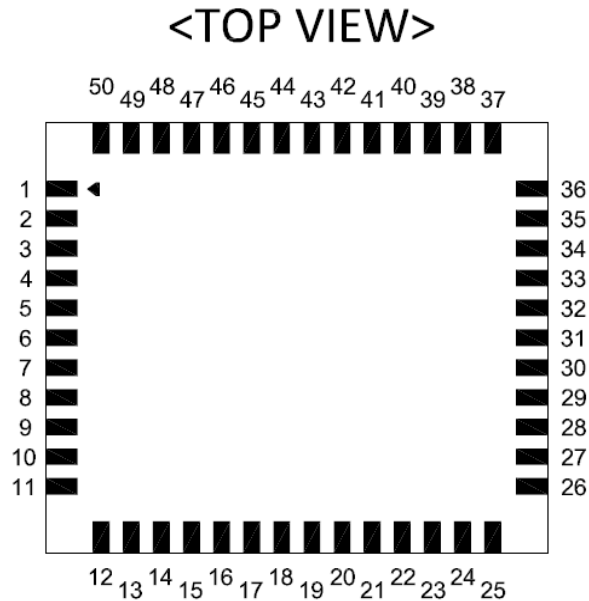
Feature	Description
General Specification	
Bluetooth Standard	BDR 、EDR(2 、3Mbps) 、LE(1Mbps 、2Mbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic 、40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	8
EDR Output Power	6
BLE Output Power	7
Sensitivity, tolerance ± 2 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-89 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-92 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-92 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-91 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).



5. Pin Definition

5.1 Pin Outline



5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	WL_BT_ANT0	I/O	RF I/O port0
3	GND	—	Ground connections
4	GND	—	Ground connections
5	GND	—	Ground connections
6	GND	—	Ground connections
7	GND	—	Ground connections
8	GND	—	Ground connections
9	WL_ANT1	I/O	RF I/O port1
10	GND	—	Ground connections
11	GND	—	Ground connections
12	PCIE_PREST_L	I	PCIe host indication to reset the device
13	XTAL_XOP	I	Xtal oscillator signal input
14	XTAL_XON	O	Xtal oscillator signal output
15	WL_REG_ON	I	Low asserting reset for WiFi core

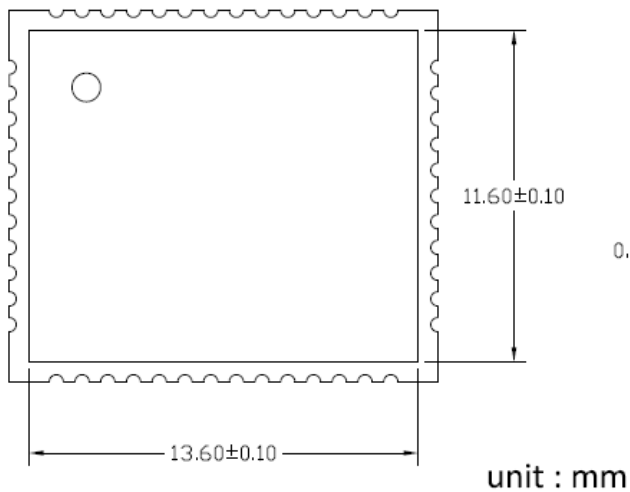


16	WL_HOST_WAKE	O	WLAN to wake-up HOST
17	NC	—	Floating (Don't connected to ground)
18	NC	—	Floating (Don't connected to ground)
19	BT_PCM_OUT	O	PCM Data output
20	BT_PCM_IN	I	PCM data input
21	BT_PCM_SYNC	I/O	PCM sync signal
22	BT_PCM_CLK	I	PCM clock
23	GND	—	Ground connections
24	PCIE_PME_L	OD	PCI power management event output
25	CBUCK_OP9	I	Internal Buck voltage generation pin
26	CSR_VLX	O	Internal Buck voltage generation pin
27	GND	—	Ground connections
28	ASR_VLX	O	Internal Analog Buck voltage generation pin
29	ABUCK_1P12	I	Internal Analog Buck voltage generation pin
30	GND	—	Ground connections
31	LPO_IN	I	External Low Power Clock input (32.768KHz)
32	GND	—	Ground connections
33	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
34	VDDIO	P	I/O Voltage supply input
35	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
36	VBAT	P	Main power voltage source input
37	PCIE_CLKREQ_L	OD	PCIe clock request
38	BT_REG_ON	I	Low asserting reset for Bluetooth core
39	GND	—	Ground connections
40	BT_UART_TXD	O	Bluetooth UART serial data output
41	BT_UART_RXD	I	Bluetooth UART serial data input
42	BT_UART_RTS_N	O	Bluetooth UART request to send
43	BT_UART_CTS_N	I	Bluetooth UART clear to send
44	PCIE_RX_N	I	PCI Express receive data-Negative
45	PCIE_RX_P	I	PCI Express receive data-Positive
46	PCIE_TX_N	O	PCI Express transmit data-Negative
47	PCIE_TX_P	O	PCI Express transmit data-Positive
48	NC	—	Floating (Don't connected to ground)
49	BT_WAKE	I	HOST wake-up Bluetooth device
50	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST

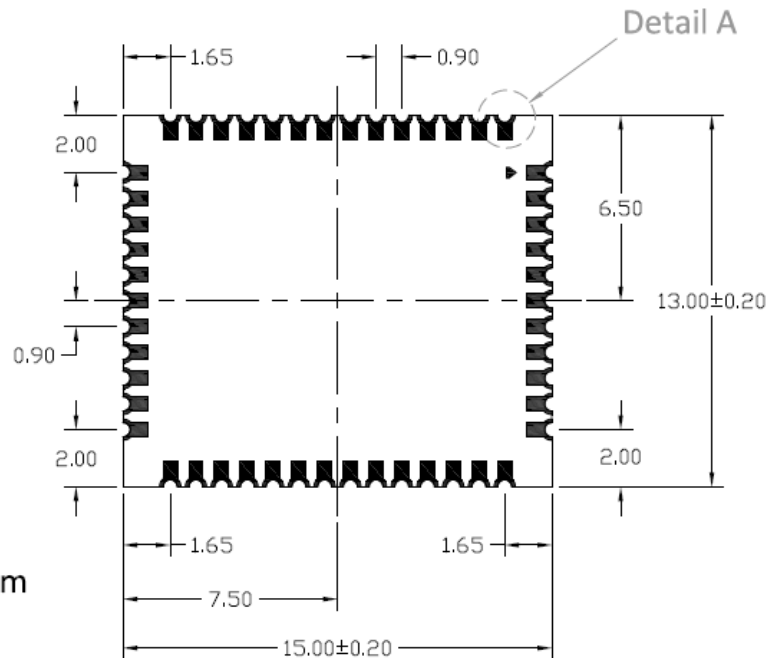
6. Dimensions

6.1 Module Dimensions

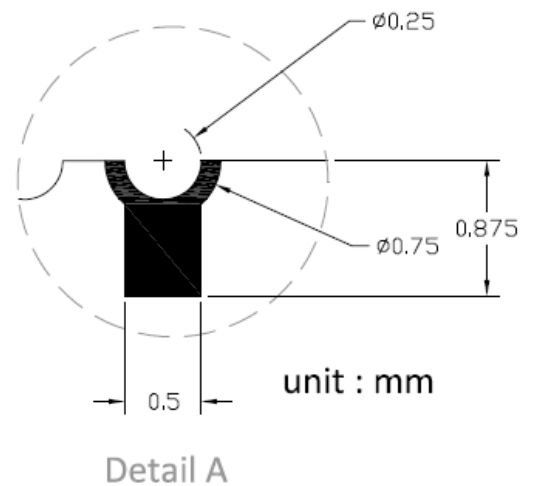
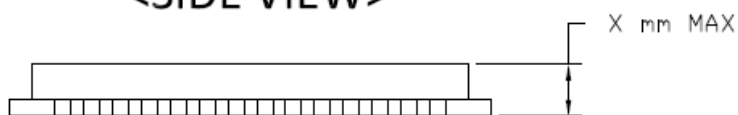
<TOP VIEW>



<BOTTOM VIEW>

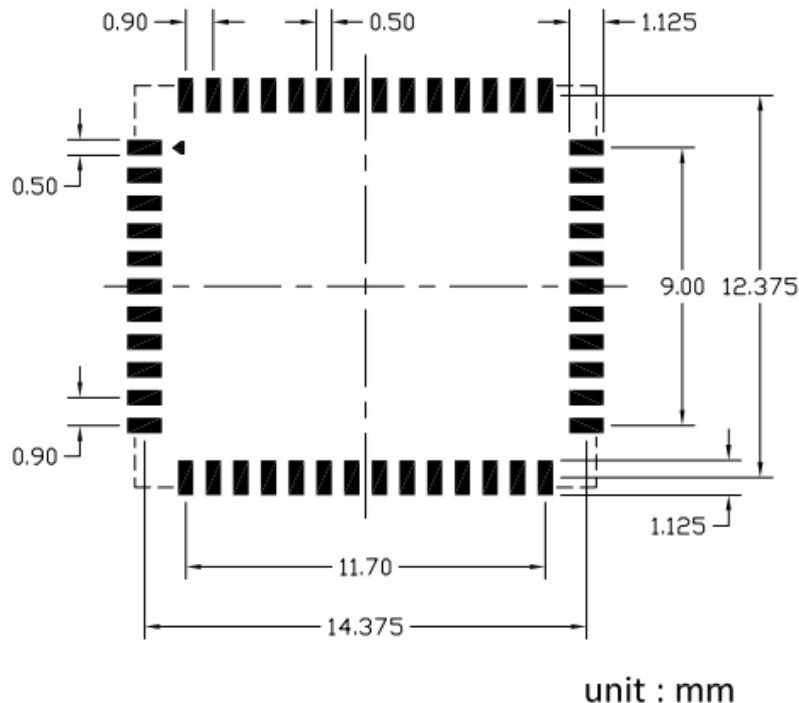


<SIDE VIEW>

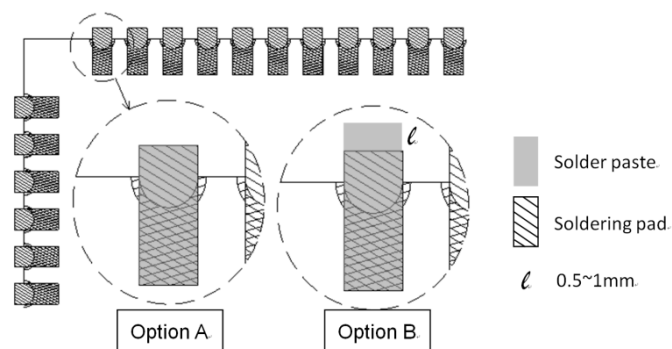


Note, X = 1.60mm

<TOP VIEW>



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

External 37.4MHz X'TAL characteristics

Parameter	Specification	Units
Nominal frequency - F ₀	37.4	MHz
Frequency Tolerance - $\Delta F / F_0$ (At 25°C +/- 3°C)	+/- 10	ppm
Operation Temperature Range - Topr	-30 ~ + 85	°C
Freq. Stability(over operating temperature) - TC Ref. to 25°C	+/- 10	ppm
Load capacitance - CL	18	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	MΩ

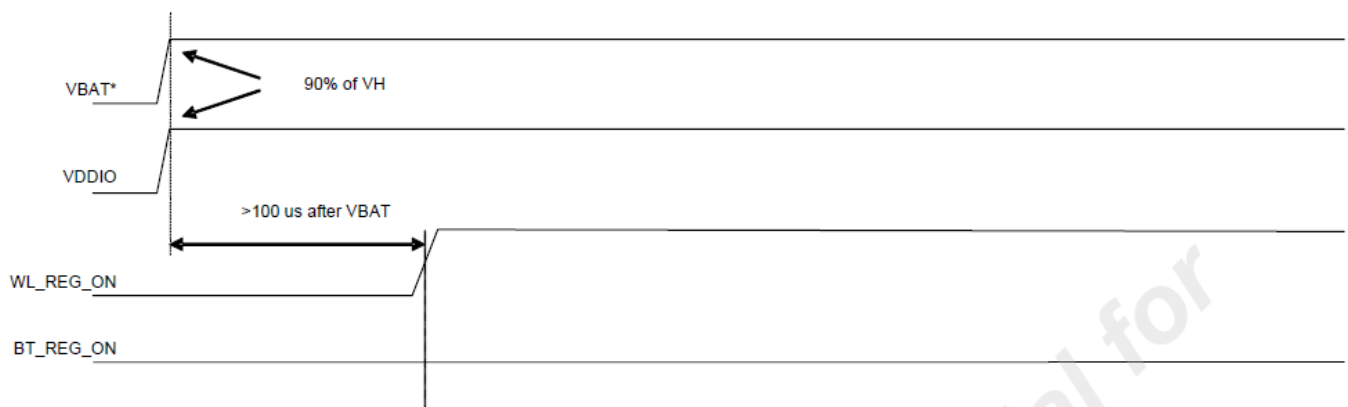
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- **WL_REG_ON**: This signal is used by the PMU to power up the WLAN section. It is also OR-gated with the **BT_REG_ON** input to control the internal regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low, the WLAN section is in reset. If **BT_REG_ON** and **WL_REG_ON** are both low, the regulators are disabled.
- **BT_REG_ON**: This signal is used by the PMU to decide whether or not to power down the internal regulators. If **BT_REG_ON** and **WL_REG_ON** are low, the regulators will be disabled.
- It suggests customers connect **WL_REG_ON** and **BT_REG_ON** to GPIOs for control, otherwise unexpected errors may occur when boot-up the device.
- In the figure, The **VDDIO** power supply has been included in the module. When **VBAT** is power-up, **VDDIO** will rise to high level after 15 ms.
- The module main chip has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after **VDDC** and **VDDIO** have both passed the POR threshold. Wait at least 150 ms after **VDDC** and **VDDIO** are available before initiating PCIe accesses.

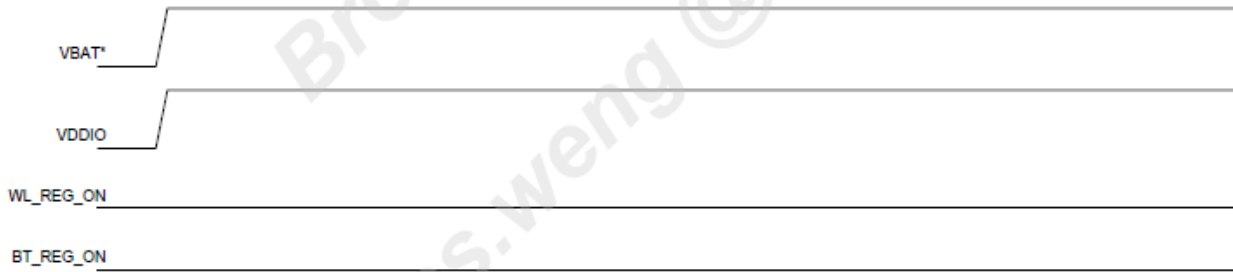


***Notes:**

1. The **VBAT** and **VDDIO** 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. **VBAT** should be up before or at the same time as **VDDIO**. **VDDIO** should NOT be present first or be held high before **VBAT** is high.

WLAN=ON, Bluetooth=ON

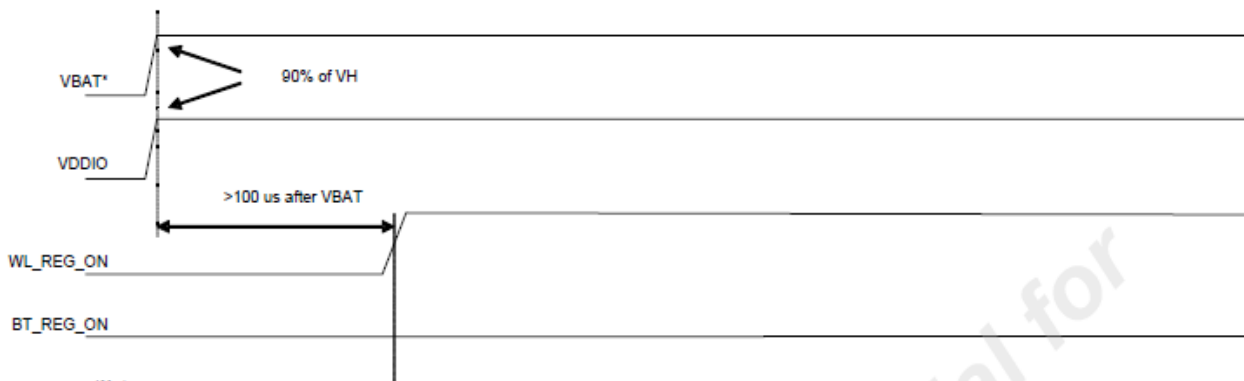




*Notes:

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

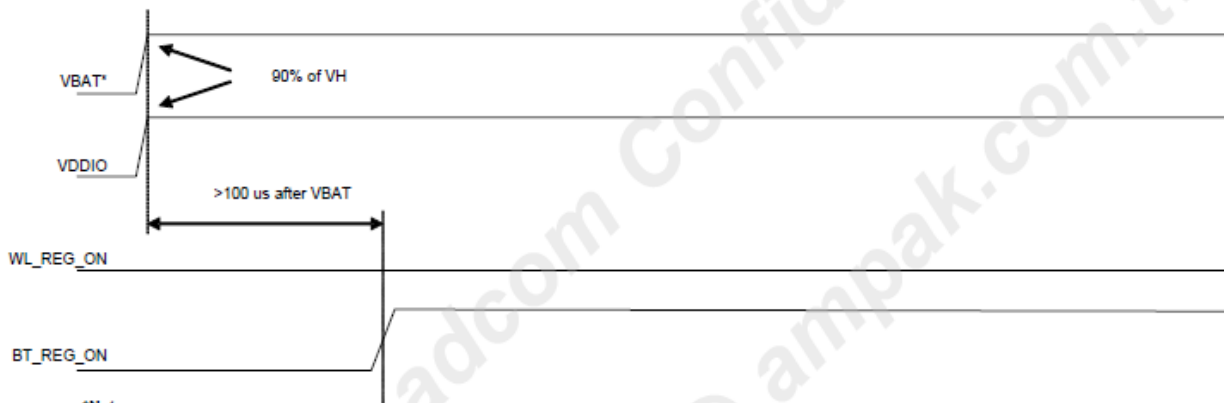
WLAN=OFF, Bluetooth=OFF



*Notes:

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=OFF



*Notes:

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=ON

8.2 PCIe Interface Description

The PCI Express(Pcie) core on the AP6398P2 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds.

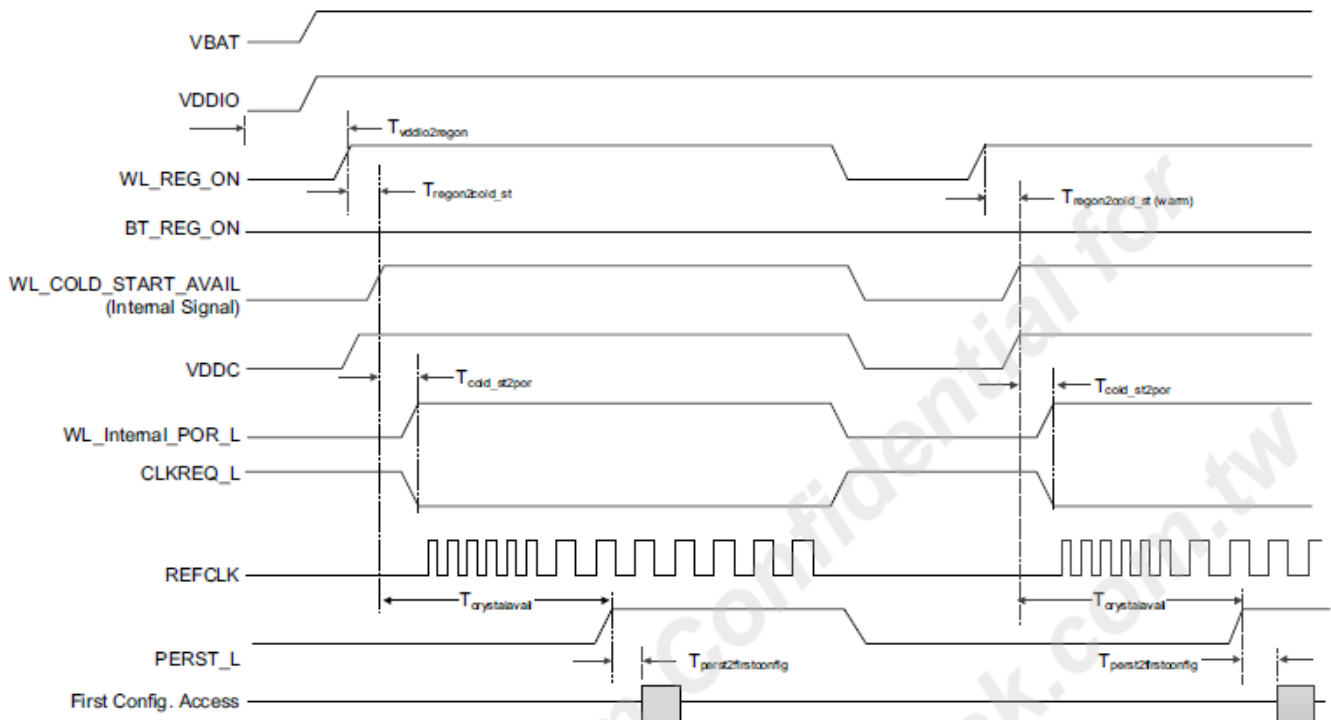
PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General^a						
Baud rate	BPS	—	—	5	—	Gbaud
Reference clock peak-to-peak differential ^b	Vref	LVPECL, AC coupled	0.95	—	—	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	—	—	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	—	—	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	—	—	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	—	—	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	—	—	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	—	—	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	—	—	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	—	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	—	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	—	—	600	mV

PCI Express Interface Parameters (Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	—	—	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	—	—	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle.	0	—	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	—	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	—	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	—	—	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	—	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	—	—	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	—	—	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	—	—	UI

PCIe Power-On Timing



Timing Parameter	Notes	Value ^a	Unit
$T_{vddio2region}$	—	0.1	ms
$T_{region2cold_st}$	3.4 ms + 162 instruction-level parallelism (ILP) cycles	10.13	ms
T_{cold_st2por}	54 ILP cycles	2.24	ms
$T_{crystalavail}$	509 ILP cycles	21.17	ms
$T_{perst2firstconfig}$	—	6.0	ms
$T_{vddioon2firstconfig}$	$T_{vddio2region} + T_{region2cold_st} + T_{crystalavail} + T_{perst2firstconfig}$	37.4 ^b	ms
$T_{region2cold_st} (warm)$	162 ILP cycles	6.73	ms

a. The time values assume an ILP tolerance of $\pm 30\%$.

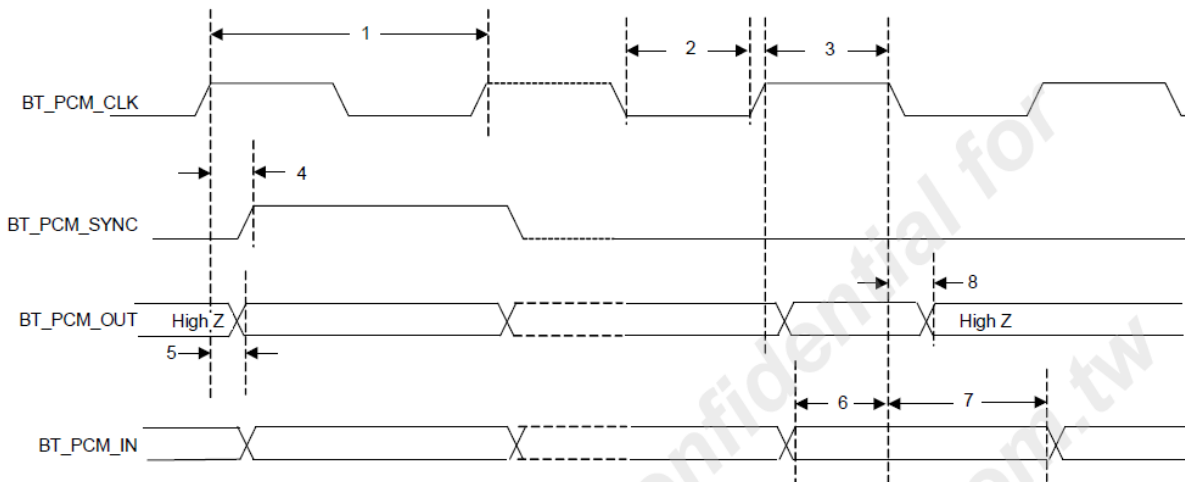
b. With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access.

8.3 PCM Interface Description

AP6398P2 supports two independent PCM interfaces that share the pins with the I²S interfaces. The PCM interface can connect to linear PCM codec devices in master or slave mode. In master mode, generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6398P2.

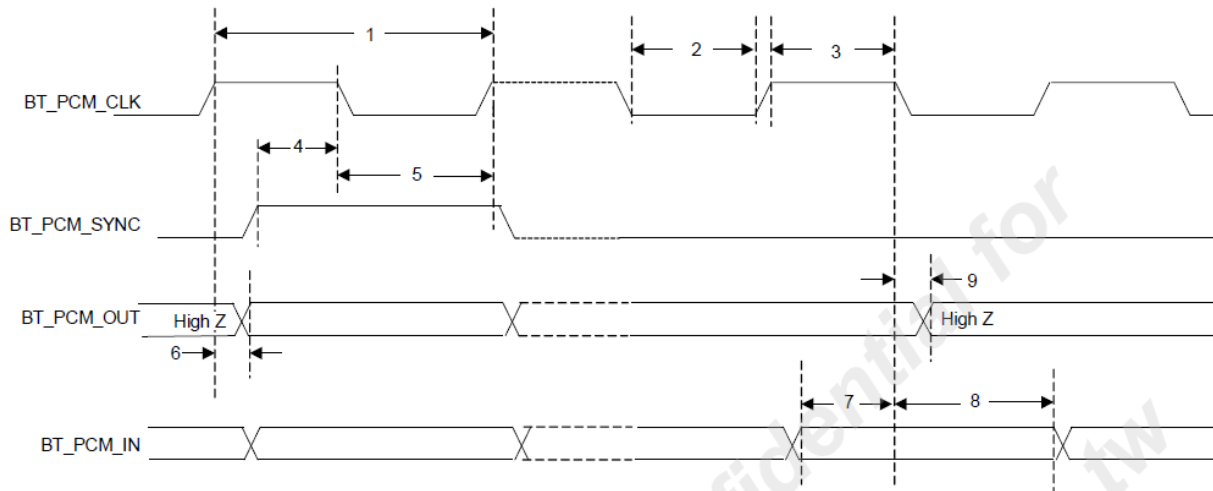
PCM Timing

Short Frame Sync, Master Mode



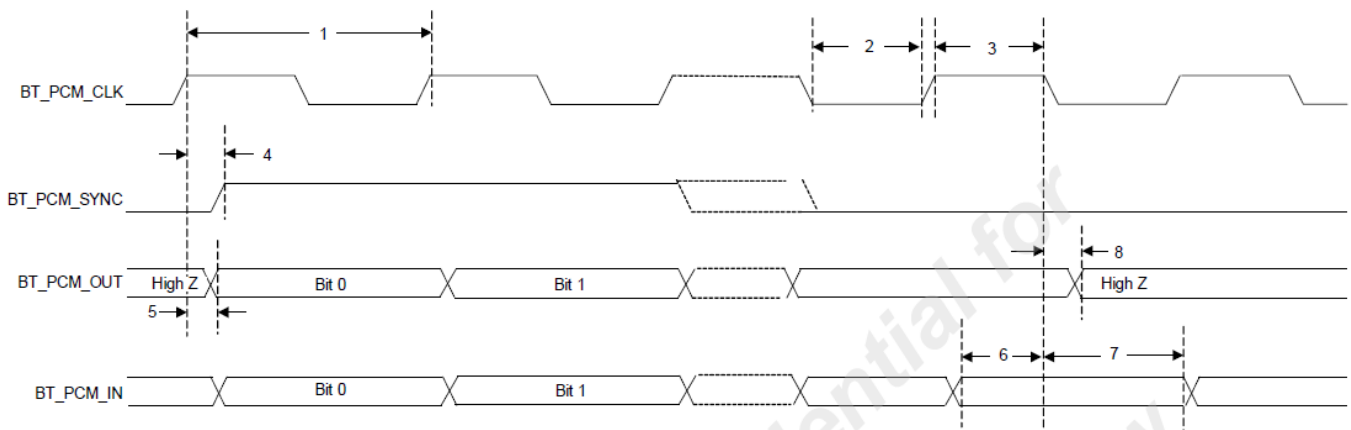
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

Short Frame Sync, Slave Mode



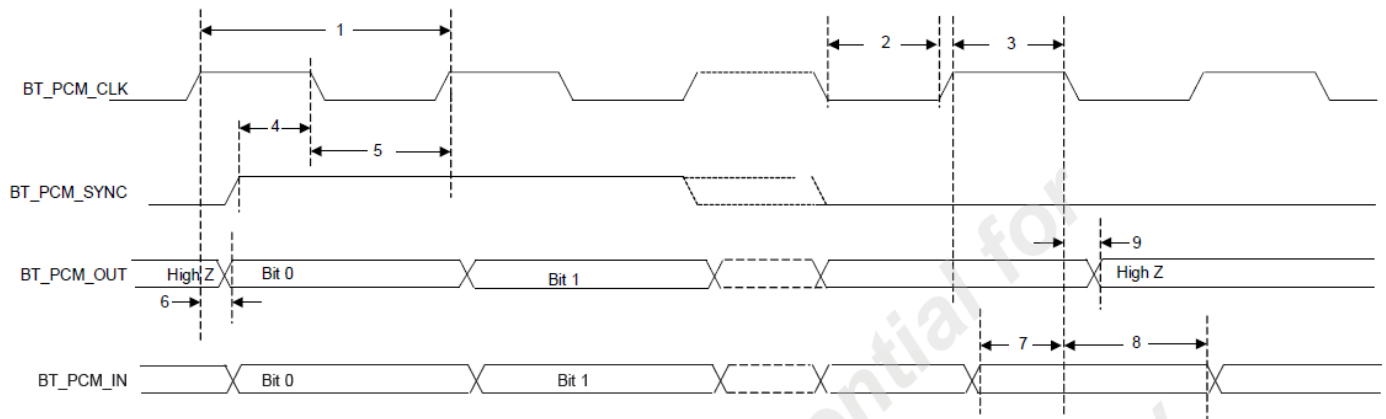
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

Long Frame Sync, Master Mode



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC delay	0	—	25	ns
5	BT_PCM_OUT delay	0	—	25	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns
8	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

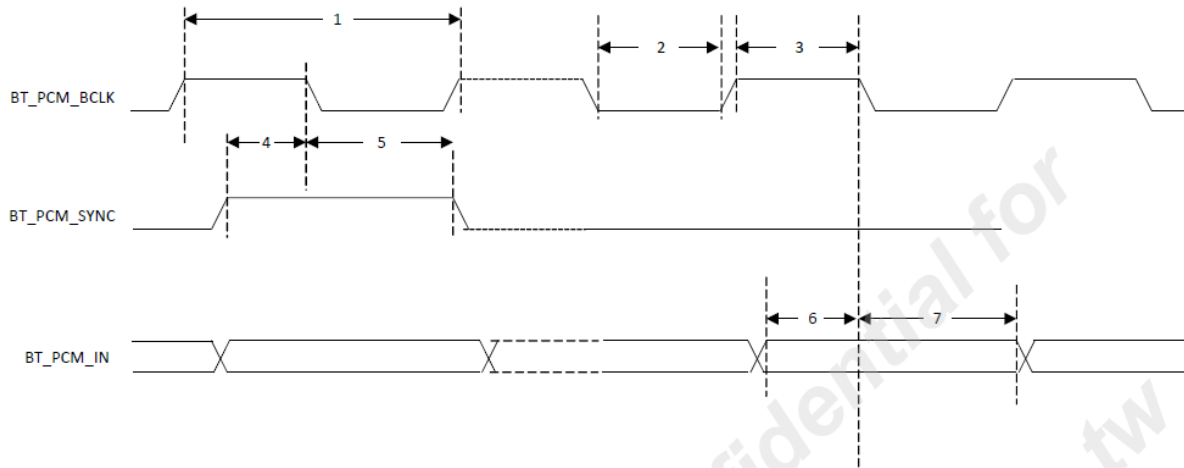
Long Frame Sync, Slave Mode



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	12	MHz
2	PCM bit clock low	41	—	—	ns
3	PCM bit clock high	41	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_OUT delay	0	—	25	ns
7	BT_PCM_IN setup	8	—	—	ns
8	BT_PCM_IN hold	8	—	—	ns
9	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	—	25	ns

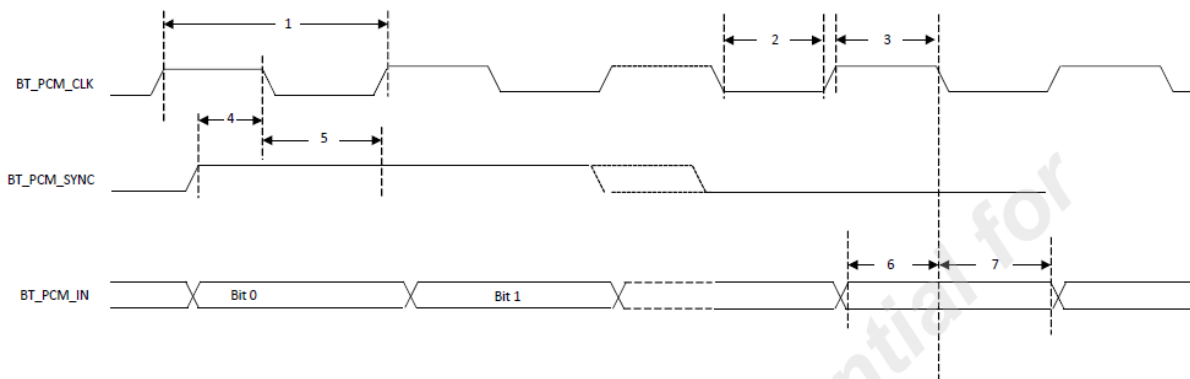
Short Frame Sync, Burst Mod





Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns

Long Frame Sync, Burst Mode



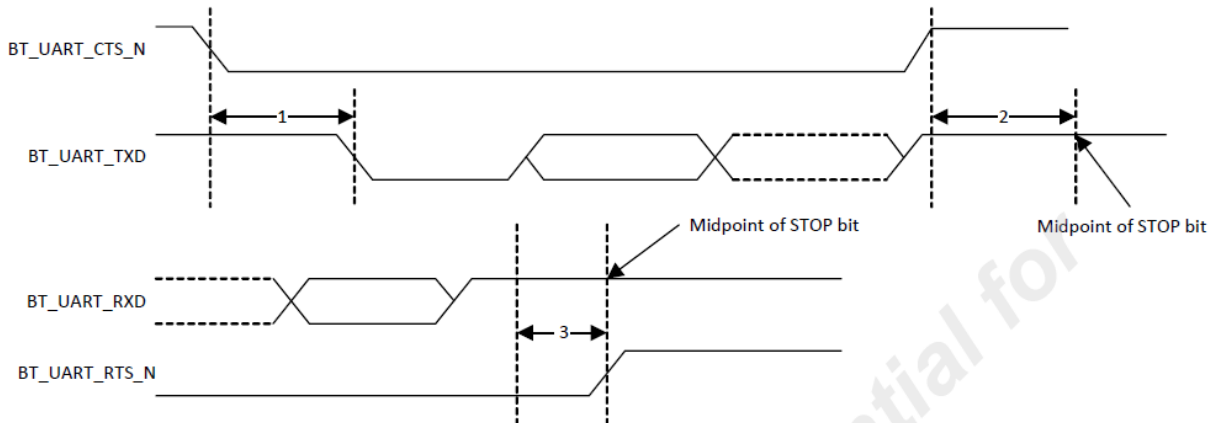
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	—	—	24	MHz
2	PCM bit clock low	20.8	—	—	ns
3	PCM bit clock high	20.8	—	—	ns
4	BT_PCM_SYNC setup	8	—	—	ns
5	BT_PCM_SYNC hold	8	—	—	ns
6	BT_PCM_IN setup	8	—	—	ns
7	BT_PCM_IN hold	8	—	—	ns



8.4 UART Interface Description

The AP6398P2 UART is a standard 4-wire interface with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

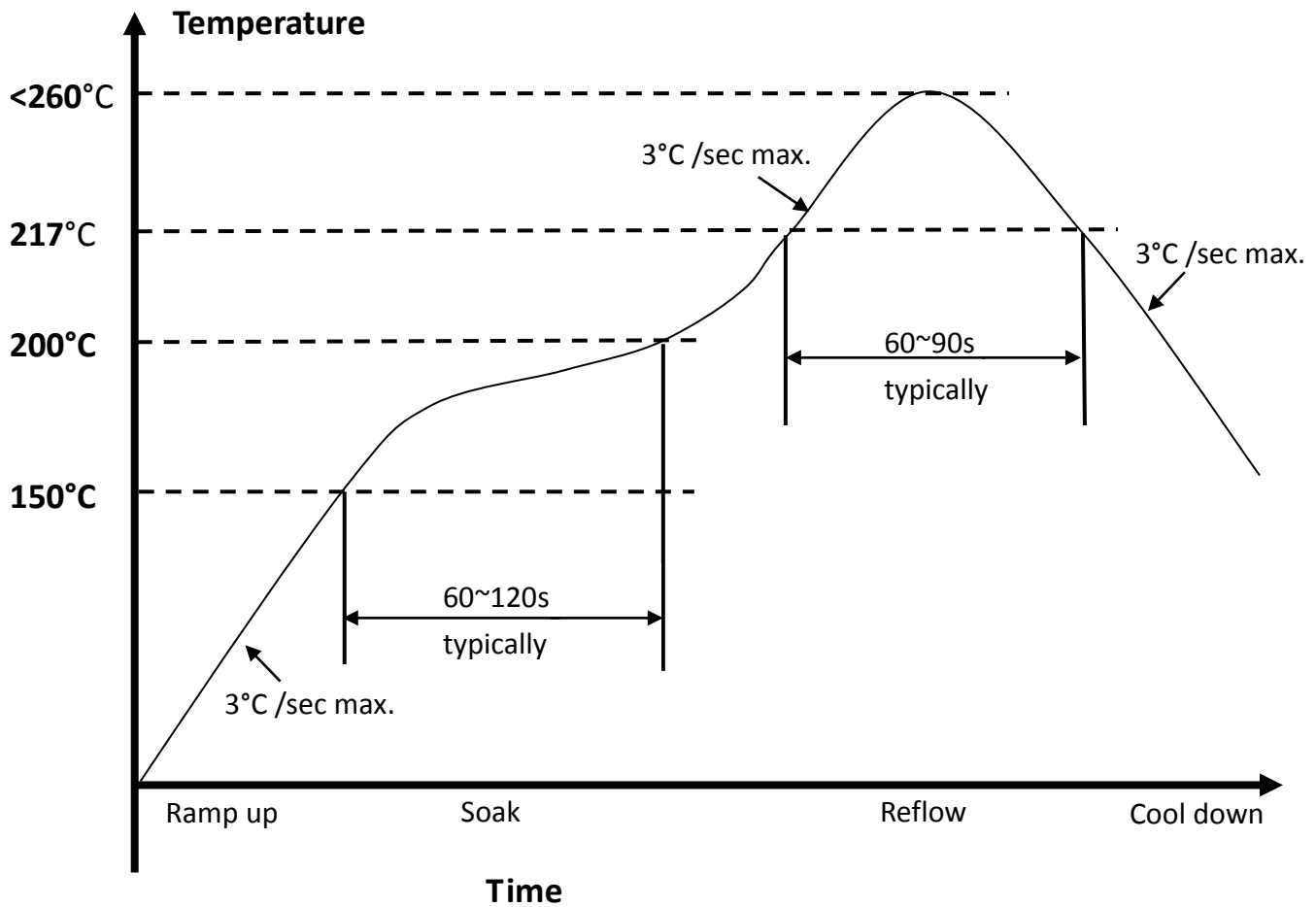
UART Timing



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods



9. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

10.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

Caution		LEVEL
This bag contains MOISTURE-SENSITIVE DEVICES		If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

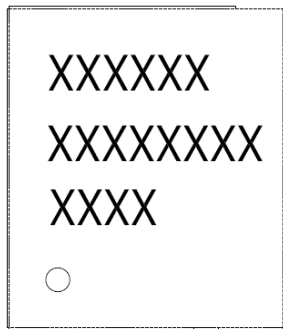
Label C → Inner box label .

PO:	_____
AMK DEVICE:	_____
PKG S/N:	9PKGYMMDDNNNNN
Model Name:	APXXXXXXX (R3HF)
P/N:	99X-XXX-XXXXR
Quantity:	1000
Date Code:	YYWW
Lot Code:	XXXXXXXX
Made in XXXXXX	

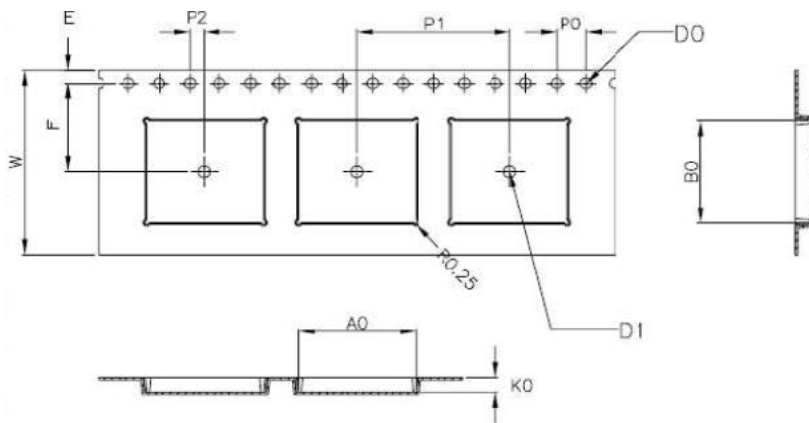
Label D → Carton box label .

AMPAK Technology Inc.	
PO:	_____
AMK DEVICE:	_____
Model Name:	APXXXXXXX (R3HF)
Part No.:	99X-XXX-XXXXR
Quantity:	5000
Lot D/C:	XXXXXXXX YYWW 5000
Manufacture:	YYYY/MM/DD
Made in XXXXXX	

10.2 Dimension

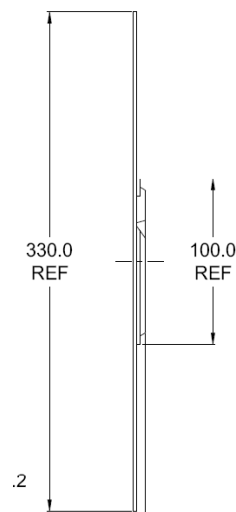
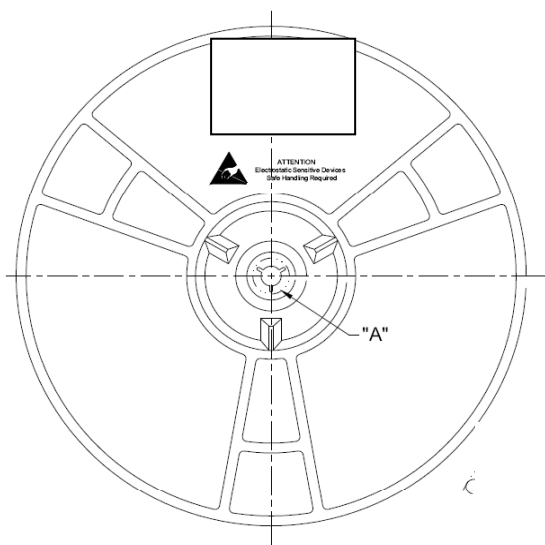


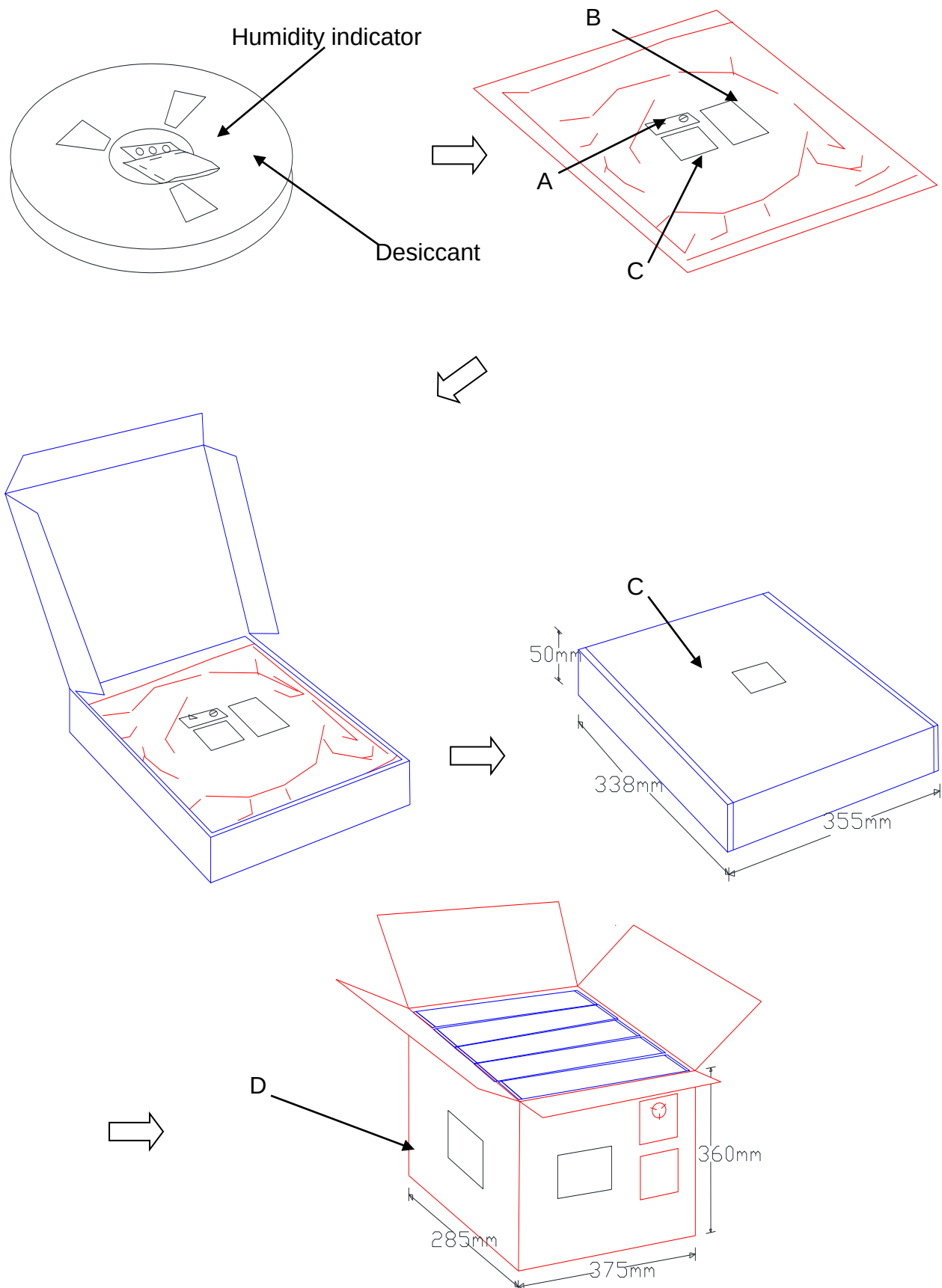
— Part Number
— Lot Code
— Date Code



W	24.00±0.30
A0	15.30±0.10
B0	13.30±0.10
K0	2.00±0.10
E	1.75±0.10
F	11.50±0.10
P0	4.00±0.10
P1	20.00±0.10
P2	2.00±0.10
D0	1.50 $\begin{smallmatrix} +0.10 \\ -0.00 \end{smallmatrix}$
D1	ø1.50MIN

1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Component load per 13" reel : 1000 pcs





10.3 MSL Level / Storage Condition

	Caution This bag contains MOISTURE-SENSITIVE DEVICES	LEVEL 4 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH) 2. Peak package body temperature: <u>250</u> $^{\circ}\text{C}$ If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: <u>72</u> hours of factory conditions If blank, see adjacent bar code label $\leq 30^{\circ}\text{C}/60\% \text{ RH}$, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$ b) 3a or 3b are not met. 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.		
Bag Seal Date: _____ If blank, see adjacent bar code label		
Note: Level and body temperature defined by IPC/JEDEC J-STD-020		