



正基科技股份有限公司

SPECIFICATION

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Customer APPROVED	
Company	
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正基科技股份有限公司



AP5875 Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2021/11/03	-- Preliminary	Ares
0.2	2022/03/15	--Modify Dimension	Ares
0.3	2022/06/08	-- Add PCIe interface information	Ares
0.4	2022/10/11	--Modify Pin define	Ares

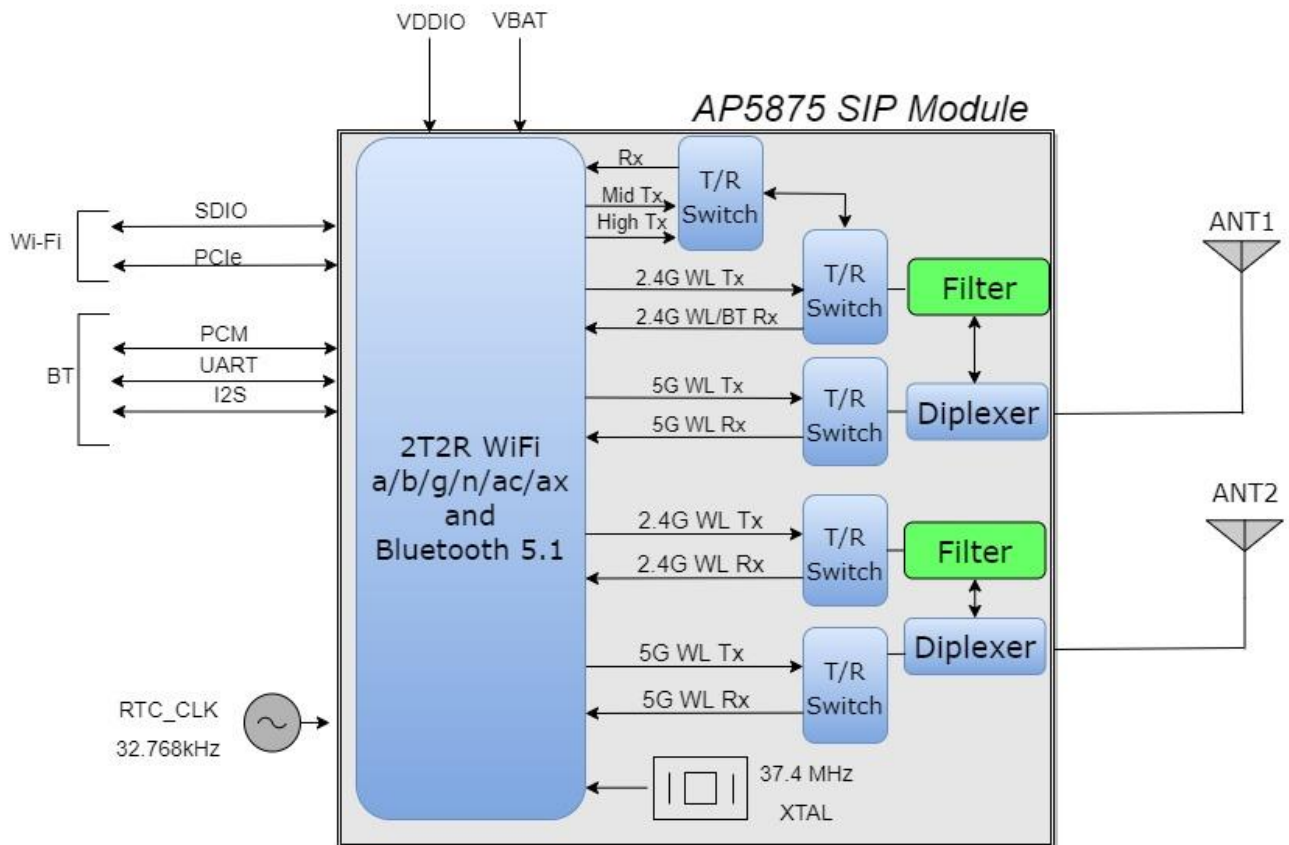
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1. Introduction

1.1 Overview

The AMPAK Technology® AP5875 is a fully Wi-Fi and Bluetooth functionalities module with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac/ax 2x2 Access Points with MIMO standard and can accomplish up to speed of 1200Mbps with dual stream in 802.11ax to connect the wireless LAN. Furthermore AP5875 included PCIe 3.0 Gen2 and SDIO v3.0 alternative interface for Wi-Fi, UART/ PCM interface for Bluetooth. In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

IEEE 802.11 Key Feature

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 1200 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (1024 QAM modulation)
- Client MU-MIMO
- Supports standard SDIO v3.0 and PCIe 3.0 Gen2, compatible with SDIO v2.0 HOST interfaces.

Bluetooth Key Feature

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
- Complies with Bluetooth Core Specification Version 5.1 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.

A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP5875
Product Description	2T2R 802.11 a/b/g/n/ac/ax Wi-Fi + BT 5.1 Module
Dimension	L x W : 10 x 10 (typical) mm , H : 1.2 (Maximum) mm
WiFi Interface	Support SDIO V3.0/2.0 and PCIe 3.0 Gen2
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.07	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.8	V
VDDIO	1.68	1.8	1.98	V

VBAT current consumption 1200mA(Peak), when VBAT = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	$0.65 \times \text{VDDIO}$	NA	V
Input low voltage	NA	$0.4 \times \text{VDDIO}$	V
Output high voltage @ 2mA	$\text{VDDIO} - 0.4$	NA	V
Output low voltage @ 2mA	NA	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11 b/g/n/ax & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11g/n：OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ax：OFDMA /256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	19	19	18	18	17
	54Mbps				
	17				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	19	19	18	17	16
	MCS7				
	16				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	19	19	18	17	16
	HE7	HE8	HE9		
	16	15	14		

802.11ax_20MHz SISO_OFDMA	Dara rate	Tones	Spec.(dBm)	Dara rate	Tones	Spec.(dBm)
	HE0	26	19	HE6	26	16
		52	19		52	16
		106	19		106	16
		242	19		242	16
	HE1~2	26	19	HE7	26	16
		52	19		52	16
		106	19		106	16

	HE3	242	19	HE8	242	16
		26	19		26	15
		52	19		52	15
		106	19		106	15
		242	19		242	15

802.11ax_20MHz SISO_OFDMA	HE4	26	18	HE9	26	14
		52	18		52	14
		106	18		106	14
		242	18		242	14
	HE5	26	17			
		52	17			
		106	17			
		242	17			

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$

802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-97		
	2Mbps	-92		
	5.5Mbps	-90		
	11Mbps	-88		
802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-84
	9Mbps	-91	36Mbps	-81
	12Mbps	-90	48Mbps	-77
	18Mbps	-87	54Mbps	-75
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-94	24Mbps	-86
	9Mbps	-93	36Mbps	-83
	12Mbps	-92	48Mbps	-79
	18Mbps	-89	54Mbps	-77
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS4	-80.5
	MCS1	-88	MCS5	-78
	MCS2	-86	MCS6	-75
	MCS3	-83	MCS7	-75

802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-79
	MCS1	-91	MCS6	-77
	MCS2	-89	MCS7	-75
	MCS3	-86	MCS8	-91.5
	MCS4	-82	MCS15	-74
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-93	HE6	-76
	HE1	-89	HE7	-76
	HE2	-87	HE8	-72
	HE3	-84	HE9	-70
	HE4	-81.5		
	HE5	-79		
802.11ax_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-92	HE6	-75
	HE1	-88	HE7	-75
	HE2	-86	HE8	-71
	HE3	-83	HE9	-69
	HE4	-81		
	HE5	-78		
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac/ax & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz （5GHz UNII Band）			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch140 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ax ： OFDMA /1024-QAM 、 256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	16.5	16.5	16.5	16.5
	5470~5720	16.5	16.5	16.5	16.5
	5725~5845	16.5	16.5	16.5	16.5
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	16.5	16		
	5470~5720	16.5	16		
	5725~5845	16.5	16		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	16.5	16.5	16.5	16.5
	5470~5720	16.5	16.5	16.5	16.5
	5725~5845	16.5	16.5	16.5	16.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	16	14.5		
	5470~5720	16	14.5		
	5725~5845	16	14.5		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14		
	5470~5720	15	14		
	5725~5845	15	14		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15.5	14.5	12.5	
	5470~5720	15.5	14.5	12.5	
	5725~5845	15.5	14.5	12.5	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15.5	14.5	12.5	11
	5470~5720	15.5	14.5	12.5	11
	5725~5845	15.5	14.5	12.5	11
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15.5	14.5	12.5	11
	5470~5720	15.5	14.5	12.5	11
	5725~5845	15.5	14.5	12.5	11
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5

802.11ax 20MHz	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15.5	14.5	12.5	12.5
	5470~5720	15.5	14.5	12.5	12.5
	5725~5845	15.5	14.5	12.5	12.5
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5720	10	10		
	5725~5845	10	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15.5	14.5	12.5	11
	5470~5720	15.5	14.5	12.5	11
	5725~5845	15.5	14.5	12.5	11
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5720	10	10		
	5725~5845	10	10		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5720	15.5	15.5	15.5	15.5
	5725~5845	15.5	15.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15.5	14.5	12.5	11
	5470~5720	15.5	14.5	12.5	11
	5725~5845	15.5	14.5	12.5	11
	Frequency (MHz)	HE10	HE11		
	5150~5350	9	9		
	5470~5720	9	9		
	5725~5845	9	9		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

802.11ax_20MHz SISO_OFDMA	Dara rate	Tones	Frequency	Spec.(dBm)
	HE0	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE1~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE3~4	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5

	HE5~7	26	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		52	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		106	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		242	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
	HE8~9	26	5150~5350	12.5
			5470~5720	12.5
			5725~5845	12.5
		52	5150~5350	12.5
			5470~5720	12.5
			5725~5845	12.5
		106	5150~5350	12.5
			5470~5720	12.5
			5725~5845	12.5
		242	5150~5350	12.5
			5470~5720	12.5
			5725~5845	12.5
	HE10~11	242	5150~5350	10
			5470~5720	10
			5725~5845	10

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_40MHz SISO_OFDMA	HE0	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE1~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5

	HE3~4	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE5~7	26	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		52	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		106	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		242	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		484	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
	HE8~9	26	5150~5350	11
			5470~5720	11
			5725~5845	11
		52	5150~5350	11
			5470~5720	11
			5725~5845	11
		106	5150~5350	11

			5470~5720	11
			5725~5845	11
		242	5150~5350	11
			5470~5720	11
			5725~5845	11
		484	5150~5350	11
			5470~5720	11
			5725~5845	11
	HE10~11	242	5150~5350	10
			5470~5720	10
			5725~5845	10
		484	5150~5350	10
			5470~5720	10
			5725~5845	10

	Dara rate	Tones	Frequency	Spec.(dBm)
802.11ax_80MHz SISO_OFDMA	HE0	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE1~2	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5

	HE3~4	26	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		52	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		106	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		242	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		484	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
		996	5150~5350	15.5
			5470~5720	15.5
			5725~5845	15.5
	HE5~7	26	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		52	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		106	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		242	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		484	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5
		996	5150~5350	14.5
			5470~5720	14.5
			5725~5845	14.5

	HE8~9	26	5150~5350	11
			5470~5720	11
			5725~5845	11
		52	5150~5350	11
			5470~5720	11
			5725~5845	11
		106	5150~5350	11
			5470~5720	11
			5725~5845	11
		242	5150~5350	11
			5470~5720	11
			5725~5845	11
		484	5150~5350	11
			5470~5720	11
			5725~5845	11
		996	5150~5350	11
			5470~5720	11
			5725~5845	11
	HE10~11	242	5150~5350	9
			5470~5720	9
			5725~5845	9
		484	5150~5350	9
			5470~5720	9
			5725~5845	9
		996	5150~5350	9
			5470~5720	9
			5725~5845	9

Sensitivity, tolerance ± 1.5 dB				
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$				
802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-86
	9Mbps	-91	36Mbps	-83
	12Mbps	-90	48Mbps	-78
	18Mbps	-89	54Mbps	-76
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-76
	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-72
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-78
	MCS1	-91	MCS6	-76
	MCS2	-89	MCS7	-75
	MCS3	-86	MCS8	-90
	MCS4	-82	MCS15	-71
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-72
	MCS3	-83	MCS8	-87
	MCS4	-79	MCS15	-68

802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-92	MCS6,NSS=1	-76
	MCS1,NSS=1	-91	MCS7,NSS=1	-75
	MCS2,NSS=1	-88	MCS8,NSS=1	-72
	MCS3,NSS=1	-85	MCS0,NSS=2	-89
	MCS4,NSS=1	-82	MCS8,NSS=2	-67
	MCS5,NSS=1	-77		
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-90	MCS6,NSS=1	-73
	MCS1,NSS=1	-88	MCS7,NSS=1	-72
	MCS2,NSS=1	-86	MCS8,NSS=1	-68
	MCS3,NSS=1	-82	MCS9,NSS=1	-66
	MCS4,NSS=1	-79	MCS0,NSS=2	-87
	MCS5,NSS=1	-77	MCS9,NSS=2	-63
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-87	MCS6,NSS=1	-70
	MCS1,NSS=1	-85	MCS7,NSS=1	-68
	MCS2,NSS=1	-82	MCS8,NSS=1	-66
	MCS3,NSS=1	-79	MCS9,NSS=1	-63
	MCS4,NSS=1	-76	MCS0,NSS=2	-84
	MCS5,NSS=1	-71	MCS9,NSS=2	-60
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-57
802.11ax_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-56
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55
802.11ax_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-87	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55

802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-53
802.11ax_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-84	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-52
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

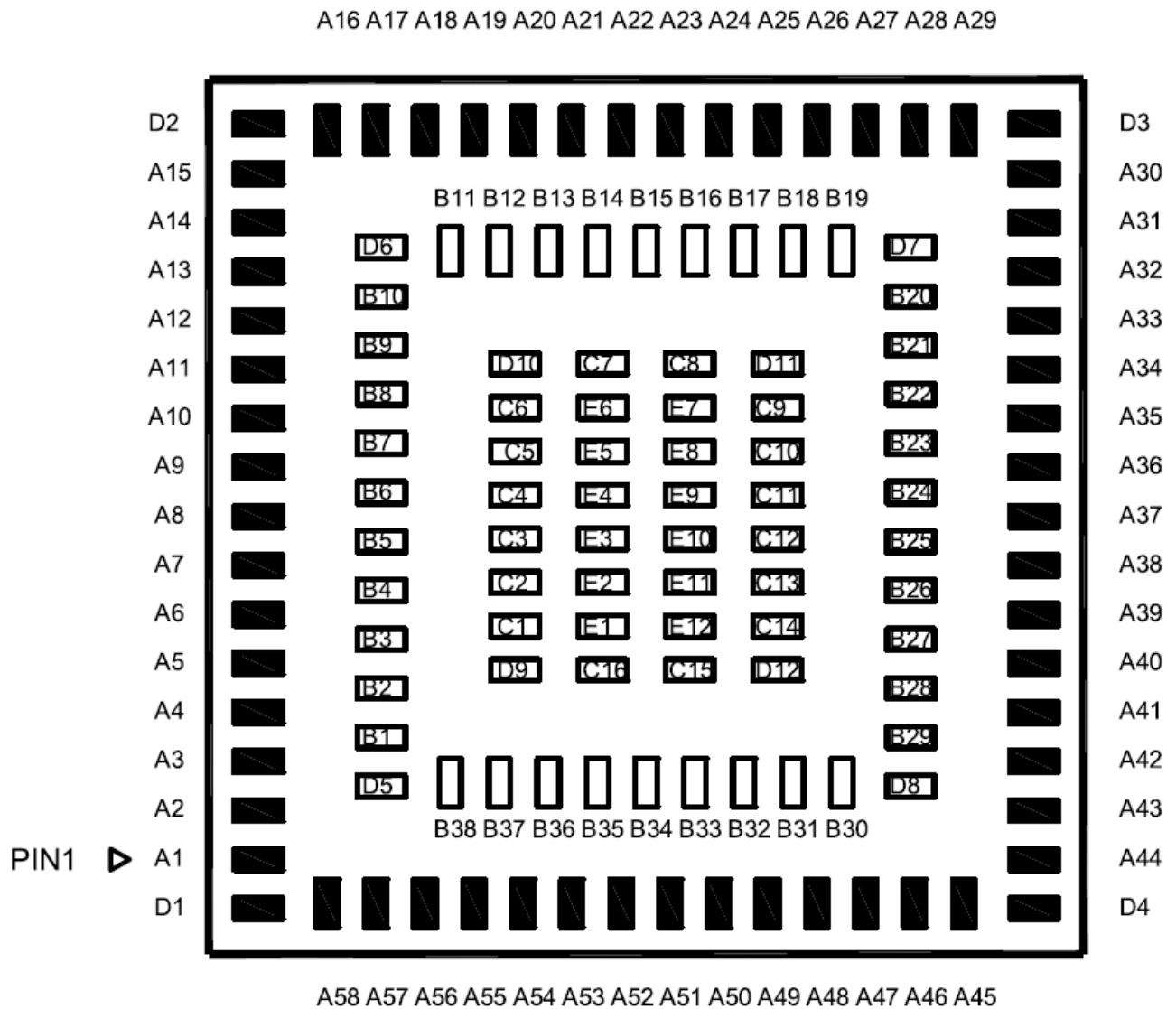
Feature	Description
General Specification	
Bluetooth Standard	BDR 、EDR(1Mbps & 2Mbps) 、LE(1Mbps) 、2LE(2Mbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic 、40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	16
EDR Output Power	9
BLE Output Power	16
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-88 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-91 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-91dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline

<TOP VIEW>



5.2 Pin Assignment

NO	Name	Type	Description
RF Port			
A54	WL_ANT0	I/O	RF I/O port0
A44	WL_ANT1	I/O	RF I/O port1
WLAN PCI Express Interface			
A19	PCIE_TX_P	O	PCI Express transmit data-Positive
A20	PCIE_TX_N	O	PCI Express transmit data-Negative
A21	PCIE_RX_N	I	PCI Express receive data-Negative
A22	PCIE_RX_P	I	PCI Express receive data-Positive
A23	PCIE_RCLK_P	I	PCI Express differential clock input-Positive
A24	PCIE_RCLK_N	I	PCI Express differential clock input-Negative
D6	PCIE_PME_L	OD	PCI power management event output
B10	PCIE_CLKREQ_L	OD	PCIe clock request
B9	PCIE_PREST_L	I	PCIe host indication to reset the device
WLAN SDIO Interface			
B12	SDIO_DATA_CMD	I/O	SDIO command line
B13	SDIO_DATA_3	I/O	SDIO data line 3
B14	SDIO_DATA_2	I/O	SDIO data line 2
B15	SDIO_DATA_1	I/O	SDIO data line 1
B16	SDIO_DATA_0	I/O	SDIO data line 0
B18	SDIO_DATA_CLK	I/O	SDIO clock line
Bluetooth UART Interface (level referred by VDDIO)			
A5	BT_UART_TXD	O	Bluetooth UART interface
A6	BT_UART_CTS_N	I	Bluetooth UART interface
A7	BT_UART_RTS_N	O	Bluetooth UART interface
A8	BT_UART_RXD	I	Bluetooth UART interface
Bluetooth PCM Interface (lever referred by VDDIO)			
A1	BT_PCM_OUT	O	BT PCM data output
A2	BT_PCM_SYNC	I/O	BT PCM sync ; can be master (output) or slave (input)
A3	BT_PCM_CLK	I/O	BT PCM CLK; can be master (output) or slave (input)
A4	BT_PCM_IN	I	BT PCM data input
Bluetooth PCM Interface (lever referred by VDDIO)			
A9	BT_I2S_DO	I/O	I2S data output
A10	BT_I2S_WS	I/O	I2S WS ; can be master (output) or slave (input)
A11	BT_I2S_CLK	I/O	I2S clock; can be master (output) or slave (input)

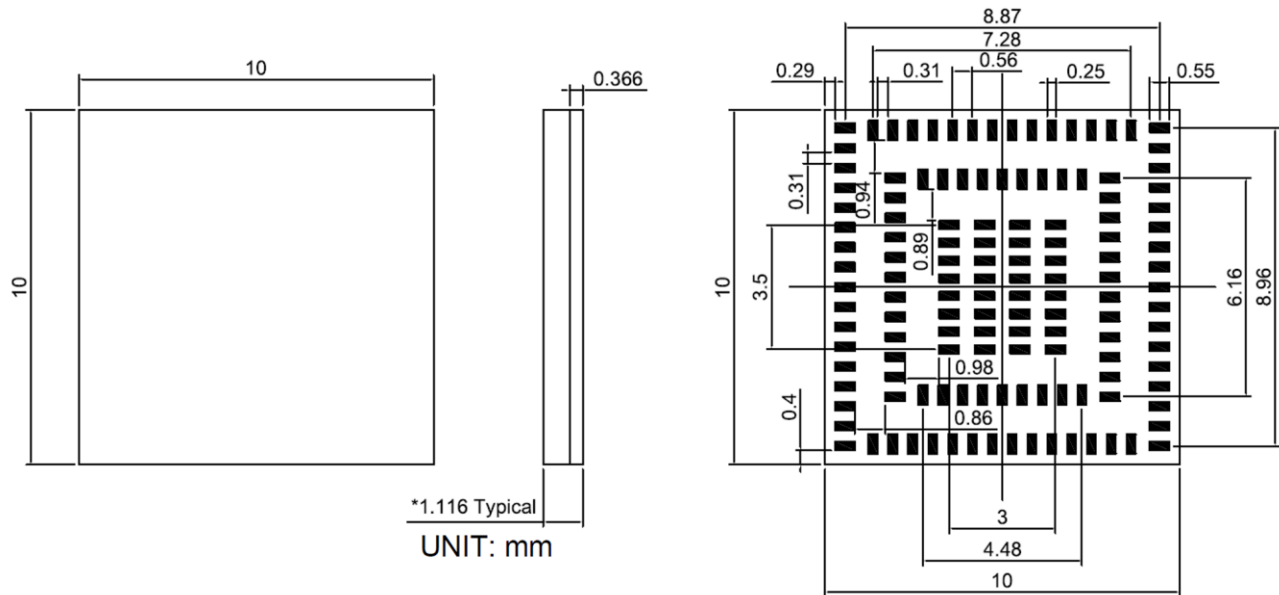
A12	BT_I2S_DI	I/O	I2S data input
Reference Clock			
C10	LPO	I	External Low Power Clock input (32.768KHz)
GPIO and Control Signal (level referred by VDDIO)			
B21	WL_HOST_WAKE	O	WLAN to wake-up HOST and WL_GPIO_0
B20	WL_DEV_WAKE	I/O	This pin can be programmed by software to be a GPIO or a WLAN_DEV_WAKE output indicating that host wake-up should be performed.
B8	DAP_SEL	I/O	This pin can be programmed to be a GPIO, the DAP_SEL signal, UART_DBG_TX or the GCI external coexistence interface. Debug access port select (DAP_SEL) 0 : Not selected 1 : Selected
B24	LTECOEX_UART_TX/ WL_UART_TX	I/O	This pin can be programmed to be a GPIO, SPI_DATA_OUT signal, UART_TX or the GCI external coexistence interface.
B25	SH_WLAN_WAKE/ WL_UART_RX	I/O	This pin can be programmed to be a GPIO, SPI_DATA_IN signal, UART_RX or the GCI external coexistence interface.
B26	DBG_UART_TX/ WL_UART_RTS	I/O	This pin can be programmed to be a GPIO, SPI_DATA_CLK signal, UART_RTS or the GCI external coexistence interface.
B27	DBG_UART_RX/ WL_UART_CTS	I/O	This pin can be programmed to be a GPIO, SPI_DATA_CS signal, UART_CTS or the GCI external coexistence interface.
A56	WL_GPIO_14	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
A57	WL_GPIO_13	I/O	This pin can be programmed to be a GPIO, DBG_UART_TX or the GCI external coexistence interface.
A58	WL_GPIO_12	I/O	This pin can be programmed to be a GPIO, DBG_UART_RX or the GCI external coexistence interface.
B7	GPIO15_SDIO_PCIE_SEL	I/O	This pin can be programmed to be a GPIO, DBG_UART_RX or the GCI external coexistence interface.
D5	BT_GPIO_2	I/O	Bluetooth general-purpose I/O
B1	BT_GPIO_3	I/O	Bluetooth general-purpose I/O
B2	GPIR_TX	I/O	Bluetooth general-purpose I/O or can be programmed to be Bluetooth IR transmit
B3	GPIR_RX	I/O	Bluetooth general-purpose I/O or can be programmed to be Bluetooth IR transmit
B5	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
B6	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
B22	BT_REG_ON	I	Low asserting reset for Bluetooth core

B23	WL_REG_ON	I	Low asserting reset for WiFi core
JTAG Interface			
A13	WL_JTAG_TRST	I/O	This pin can be programmed to be a GPIO, the JTAG TRST signal, DBG_UART_RX or the GCI external coexistence interface.
A14	SH_UART_TX/WL_JTAG_TMS	I/O	This pin can be programmed to be a GPIO, the JTAG TMS signal, UART_TX or the GCI external coexistence interface.
A15	SH_WAKE/WL_JTAG_TDO		This pin can be programmed to be a GPIO, the JTAG TDO signal, UART_TRTS or the GCI external coexistence interface.
A16	SH_UART_RX/WL_JTAG_TCK		This pin can be programmed to be a GPIO, the JTAG TCK signal, UART_RX or the GCI external coexistence interface.
A17	LTECOEX_UART_RX/ WL_JTAG_TDI		This pin can be programmed to be a GPIO, the JTAG TDI signal, UART_CTS or the GCI external coexistence interface.
C12	JTAG_SEL	I/O	JTAG select. This pin must be connected to ground if the JTAG interface is not used.
Power Supplies			
A33	VBAT	P	Main power voltage source input
A34			
A39	VDDIO	P	I/O Voltage supply input
A40			
A29	CSR_VLX	O	Internal Buck voltage generation pin
A27	CBUCK_OP9	I	Internal Buck voltage generation pin
A30	ASR_VLX	O	Internal Analog Buck voltage generation pin
A31			
A36	ABUCK_1P12	I	Internal Analog Buck voltage generation pin
A37			
Ground			
A18	GND	-	Ground
A25		-	
A26		-	
A28		-	
A32		-	
A35		-	
A38		-	

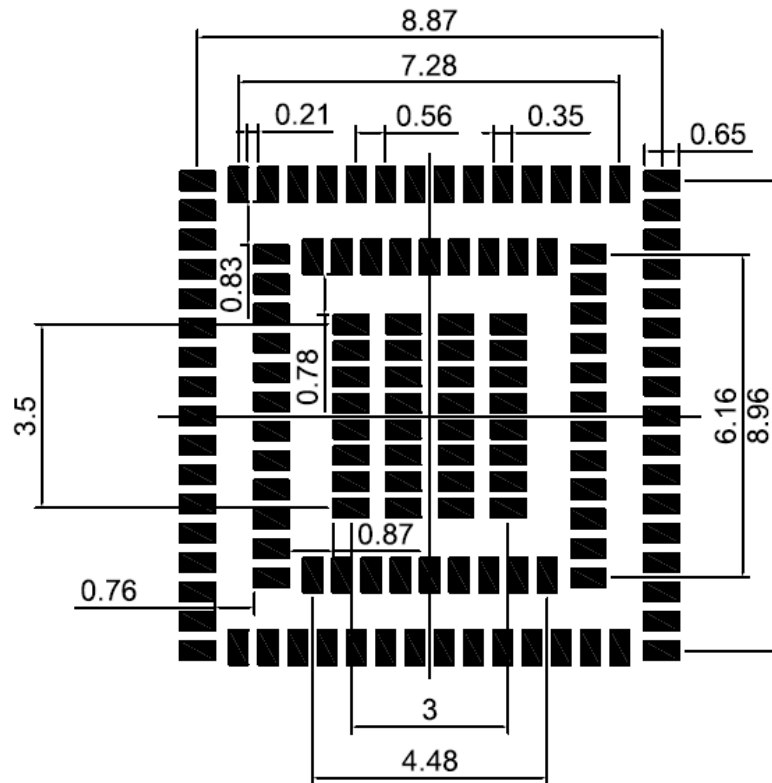
A41-43	GND	-	Ground
A45-A53		-	
A55		-	
B4		-	
B11		-	
B17		-	
B19		-	
B28-B38		-	
C1-C9		-	
C11		-	
C13-C14		-	
D1-D4		-	
D7-D12		-	
E1-E12		-	

6. Dimensions

6.1 Module Dimensions



<TOP VIEW>



- Solder paste layer design is generally the same as recommended footprint.
(錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
(如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計，或是聯絡正基科技技術支持團隊)。

7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

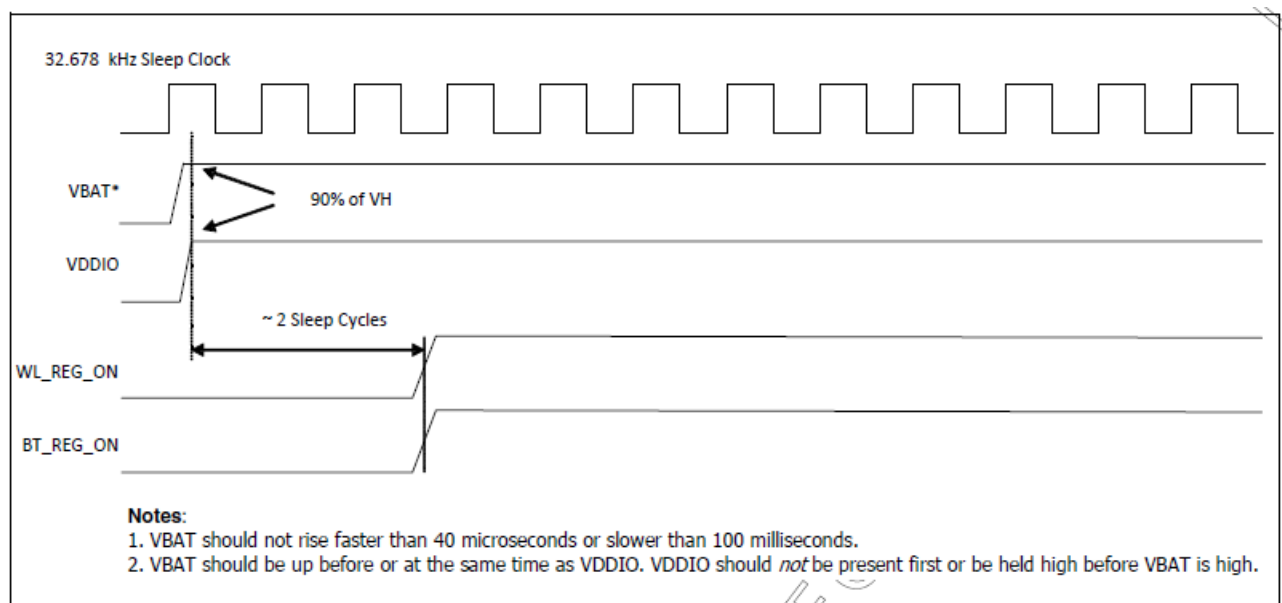
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

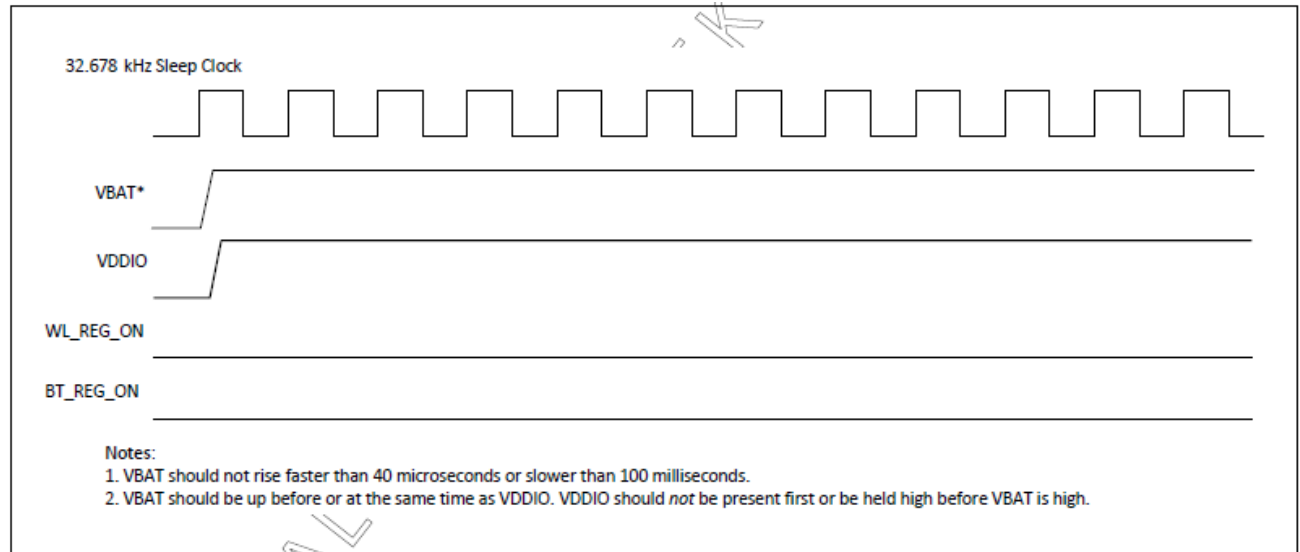
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

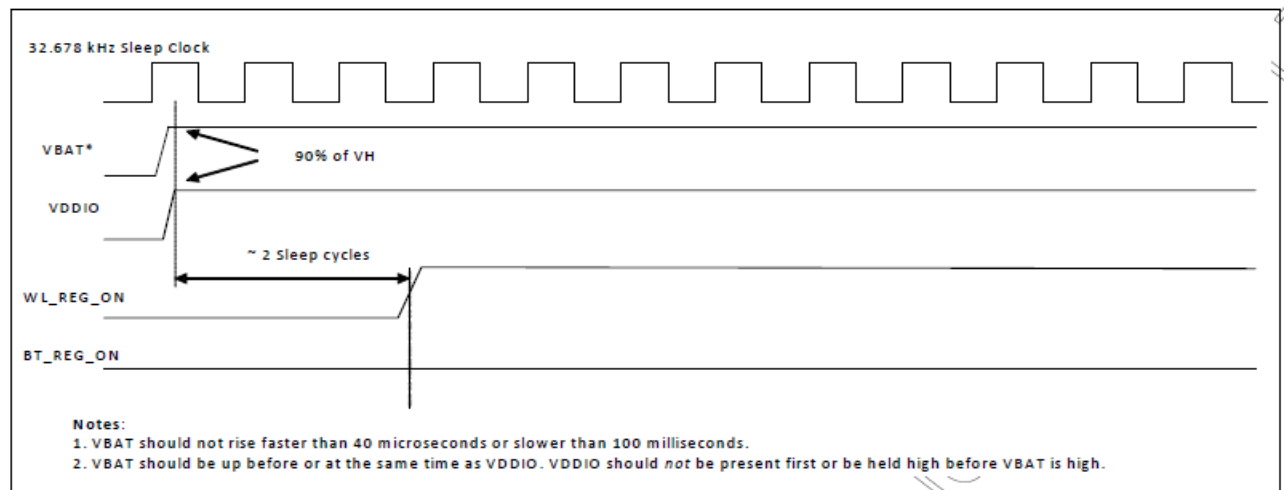
- **WL_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



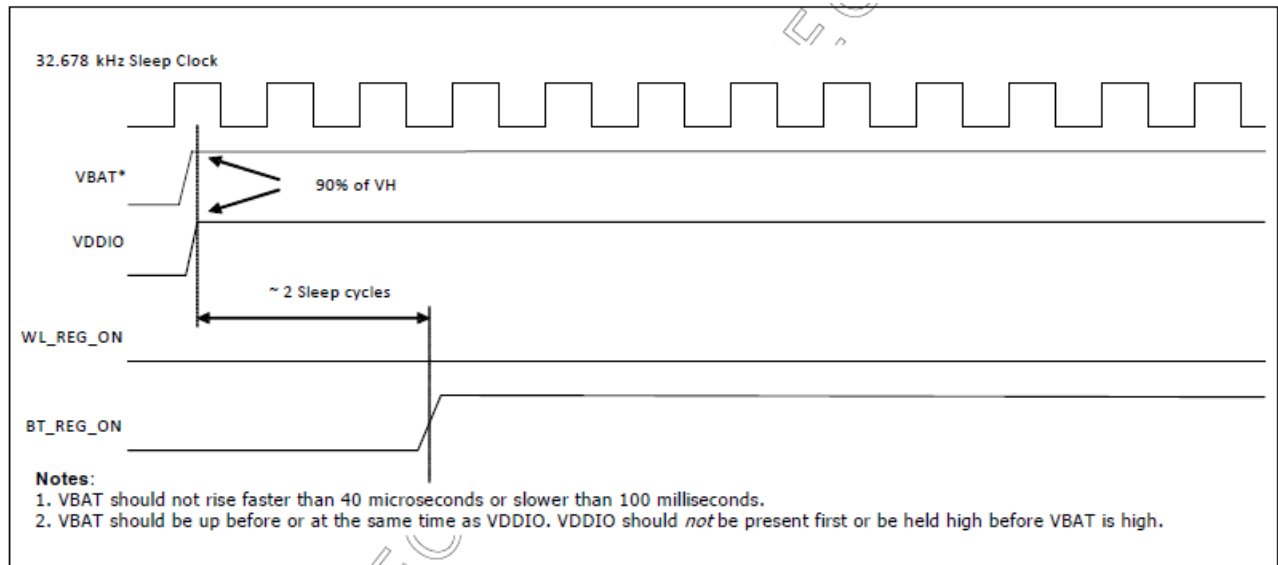
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

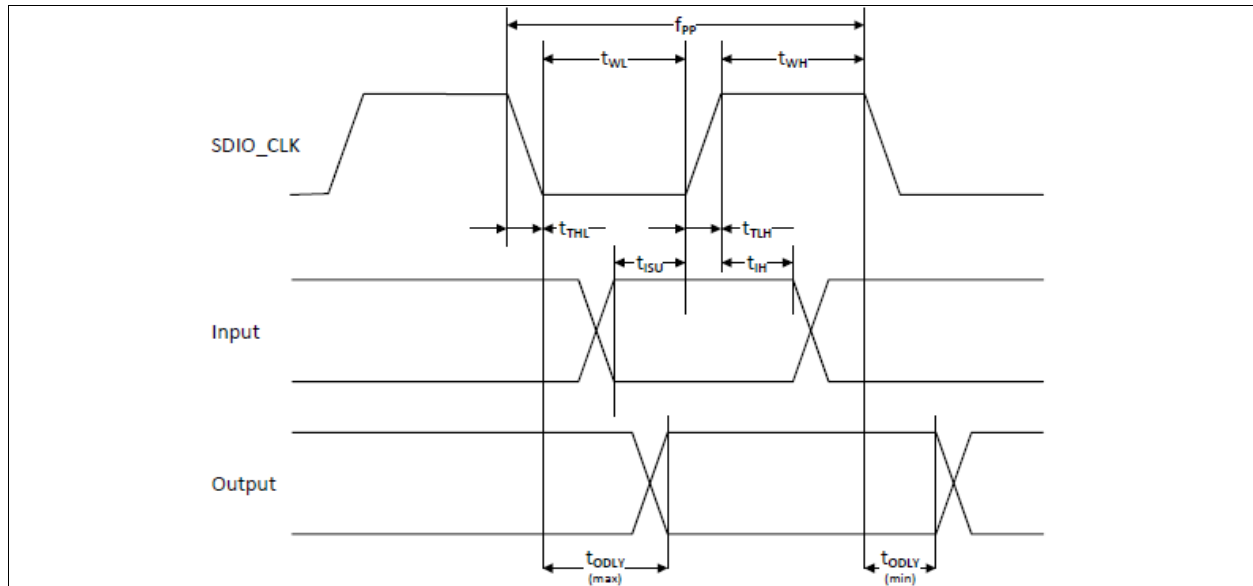
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps), SDR104(208MHz) and DDR50(50MHz, dual rates). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

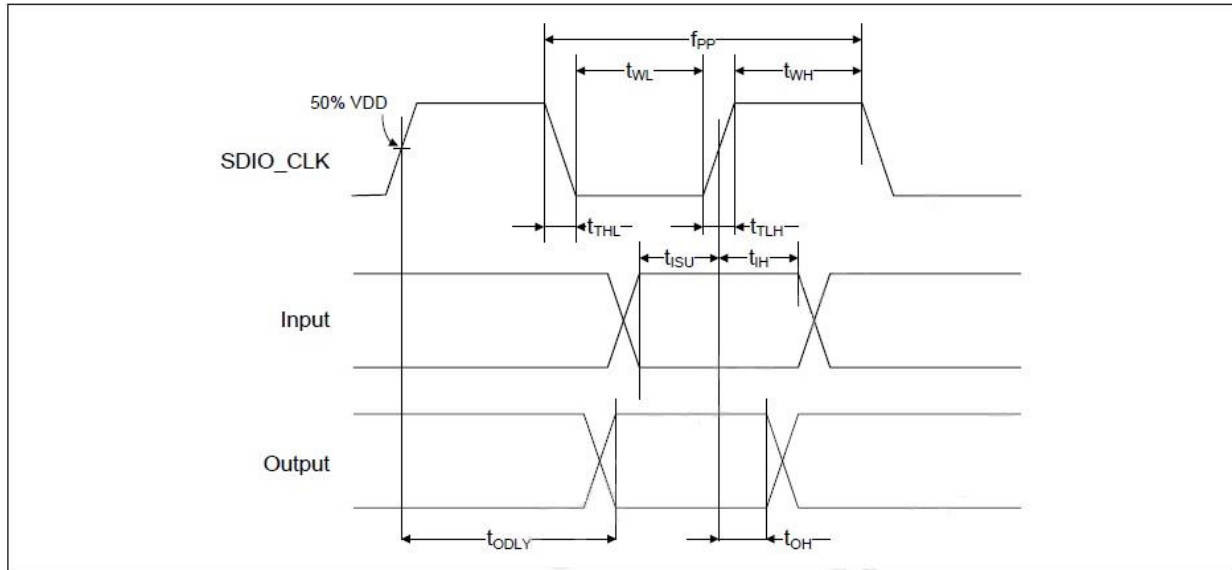
SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

- a. Timing is based on $CL \leq 40pF$ load on CMD and Data.
 b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

SDIO High Speed Mode Timing Diagram



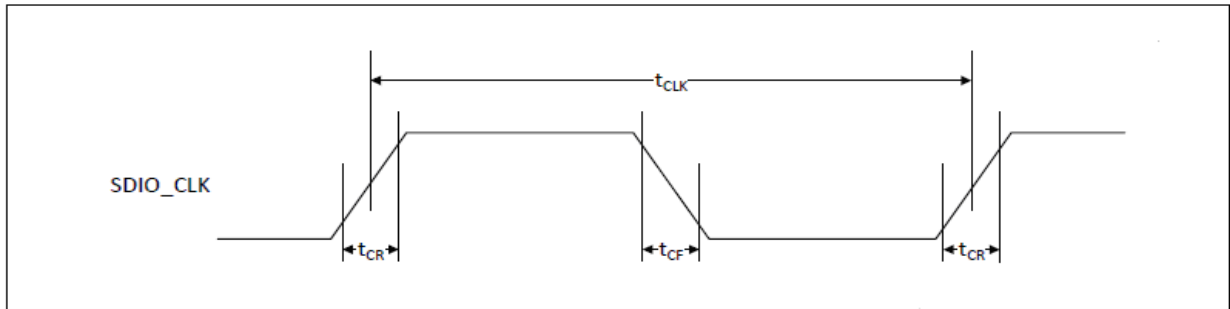
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f_{pp}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on $CL \leq 40$ pF load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

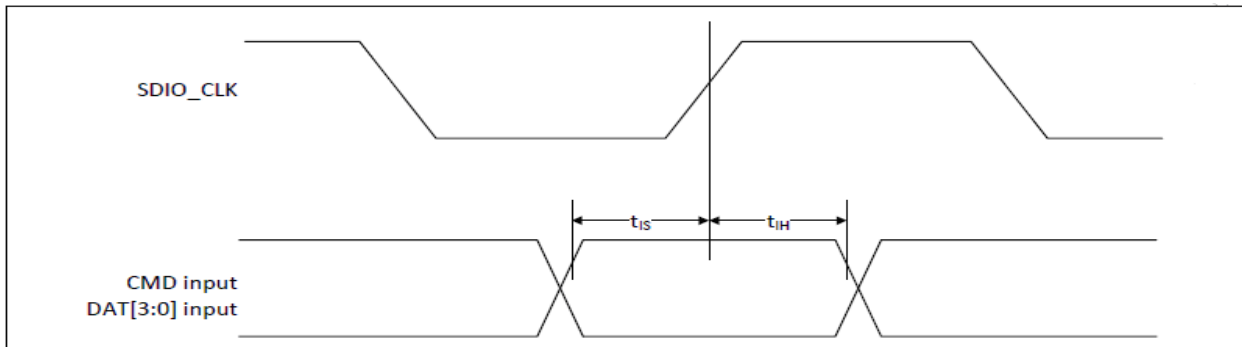
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



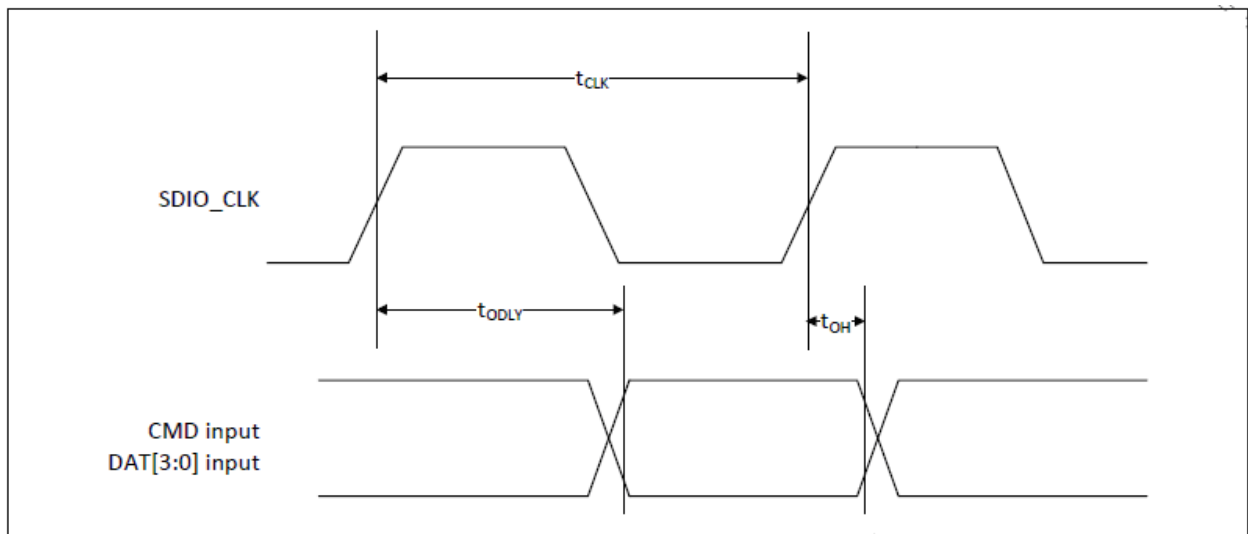
Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	40	—	ns	SDR12 mode
		20	—	ns	SDR25 mode
		10	—	ns	SDR50 mode
		4.8	—	ns	SDR104 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	—	30	70	%	—

SDIO Bus Input timing (SDR Modes)



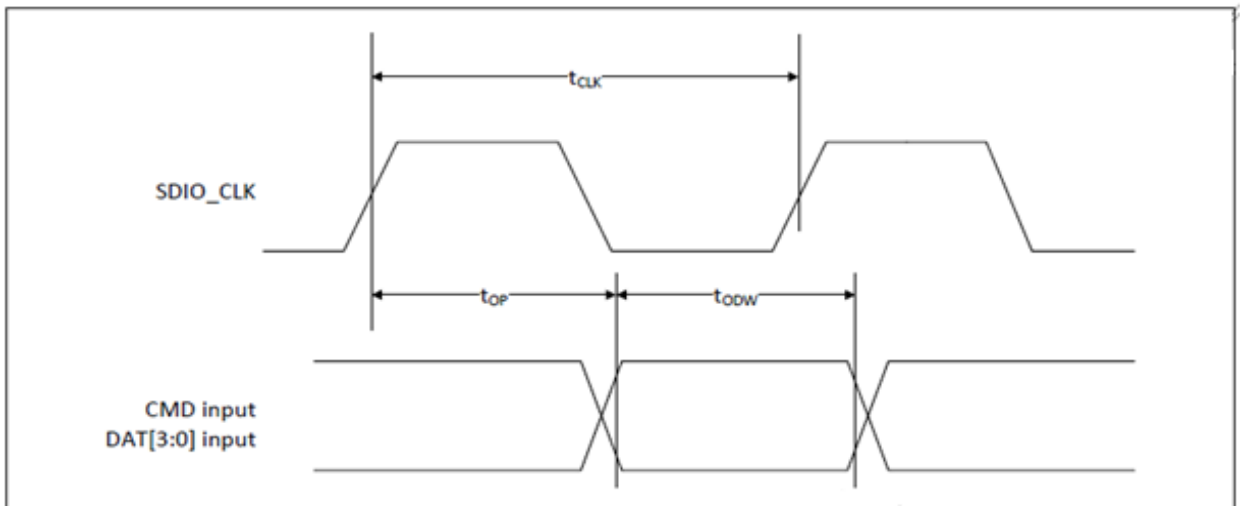
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	—	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	—	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	—	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	—	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

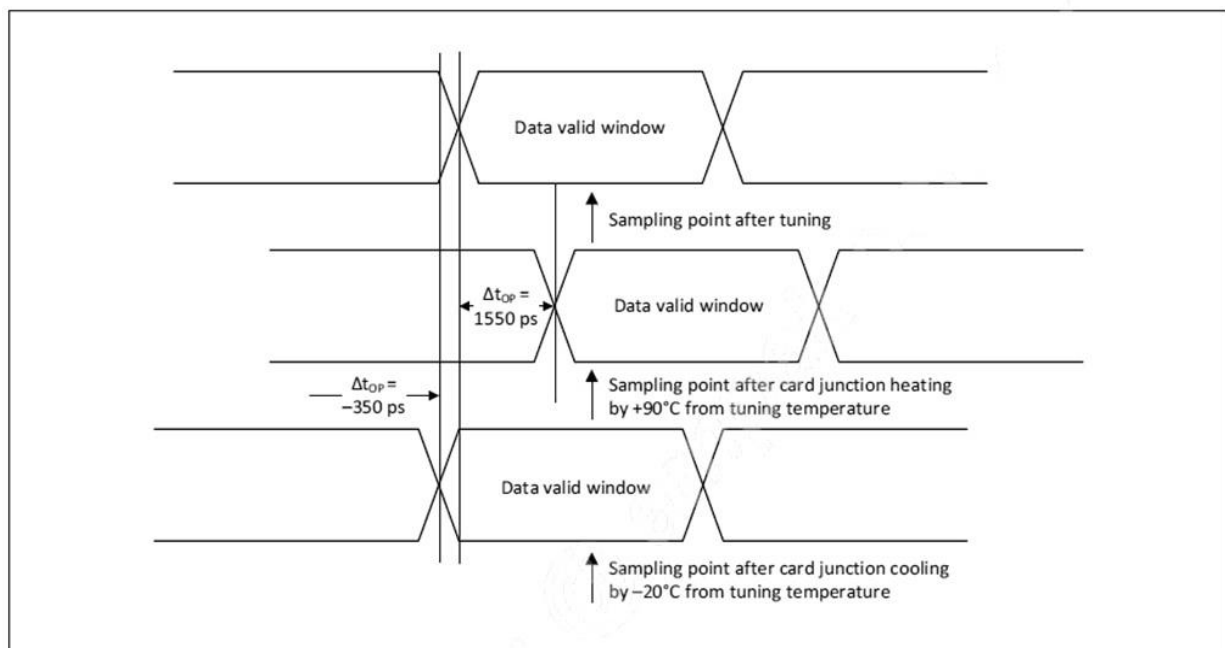
Card output timing (SDR Modes 100MHz to 208MHz)



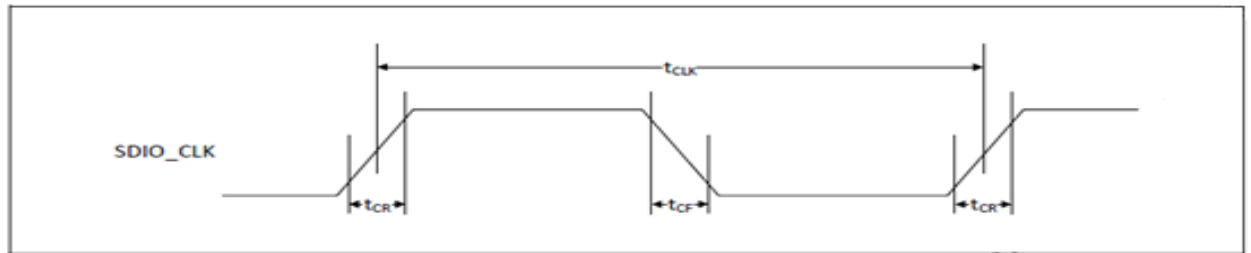
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	—	UI	$t_{ODW}=2.88$ ns @208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

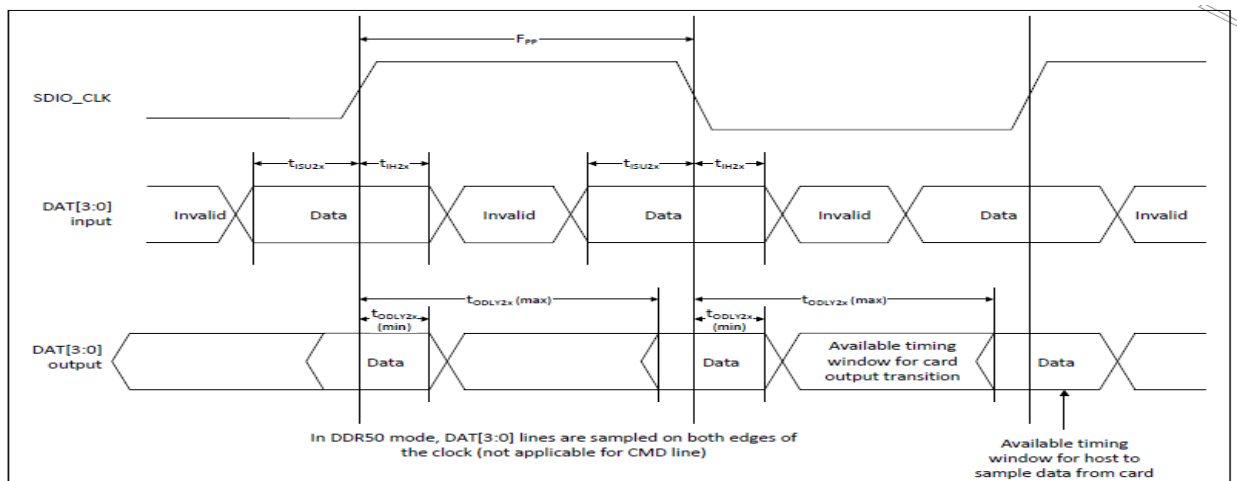


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	—	45	55	%	—

Data Timing



Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30$ pF (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25$ pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)

8.3 PCIe Interface Description

The PCI Express(Pcie) core on the AP5876 is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen1 speeds.

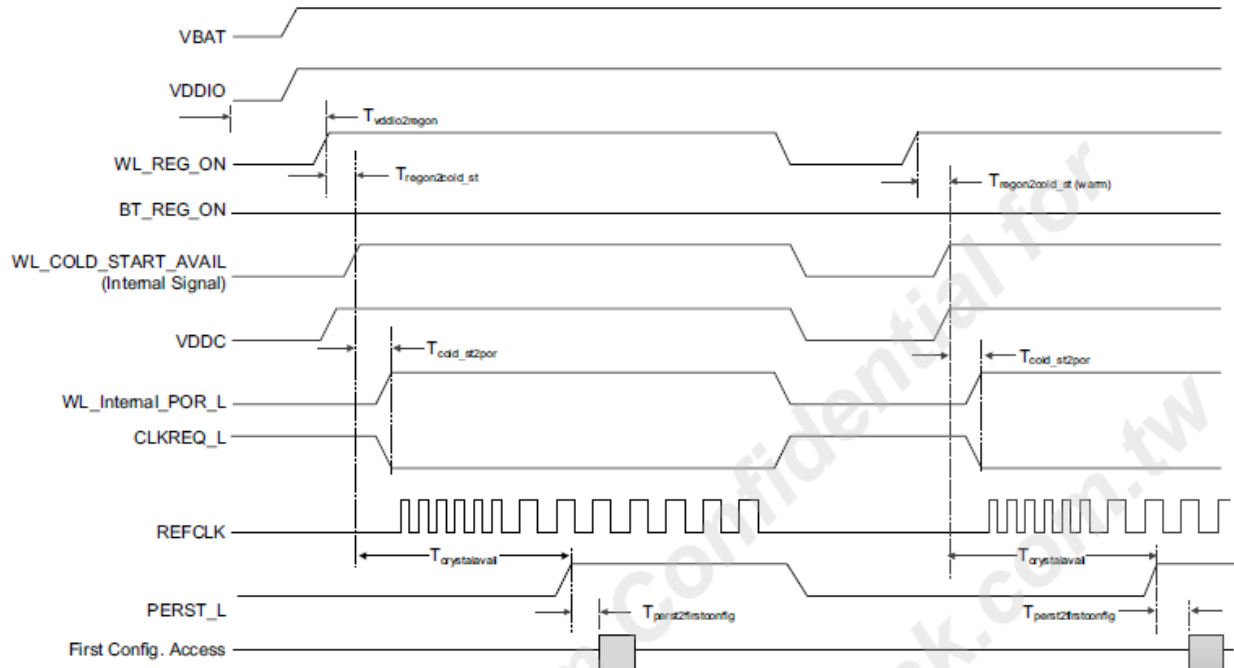
PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General^a						
Baud rate	BPS	—	—	5	—	Gbaud
Reference clock peak-to-peak differential ^b	Vref	LVPECL, AC coupled	0.95	—	—	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100k	—	—	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1k	—	—	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	—	—	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	—	—	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	—	—	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	—	—	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	—	—	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	—	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	—	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	—	—	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	—	—	600	mV

PCI Express Interface Parameters (Continued)

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	—	—	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	—	—	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electrical idle.	0	—	100	mV
Absolute delta of DC common-mode voltage between D+ and D-	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D-	0	—	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	—	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	—	—	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	—	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min) for 0.05: 1.25 GHz	—	—	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	—	—	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	—	—	UI

PCIe Power-On Timing



Timing Parameter	Notes	Value ^a	Unit
$T_{vddio2region}$	–	0.1	ms
$T_{region2cold_st}$	3.4 ms + 162 instruction-level parallelism (ILP) cycles	10.13	ms
T_{cold_st2por}	54 ILP cycles	2.24	ms
$T_{crystalavail}$	509 ILP cycles	21.17	ms
$T_{perst2firstconfig}$	–	6.0	ms
$T_{vddioon2firstconfig}$	$T_{vddio2region} + T_{region2cold_st} + T_{crystalavail} + T_{perst2firstconfig}$	37.4 ^b	ms
$T_{region2cold_st} (warm)$	162 ILP cycles	6.73	ms

a. The time values assume an ILP tolerance of $\pm 30\%$.

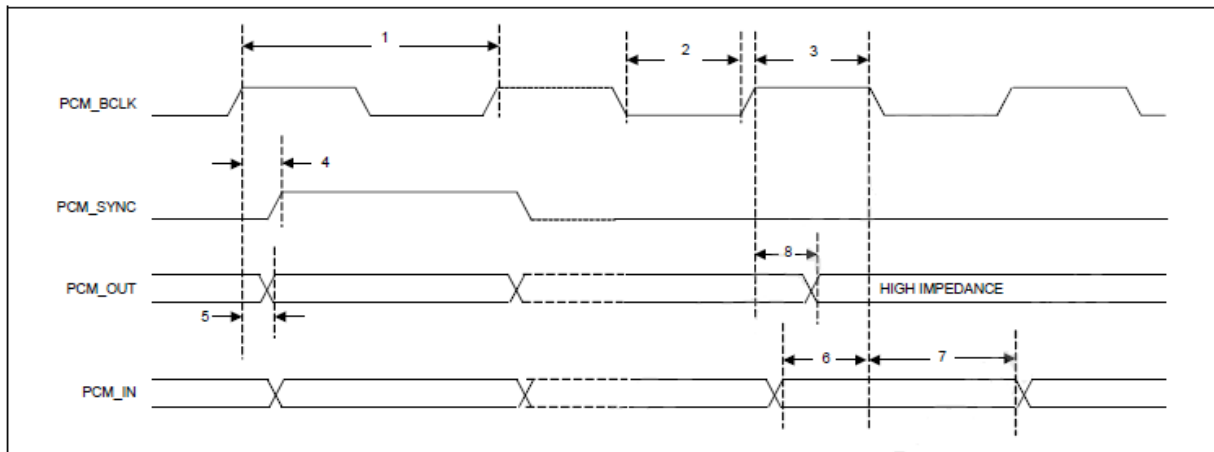
b. With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access.

8.4 PCM Interface Description

The PCM Interface on the AP6275S can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6275S generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6275S. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

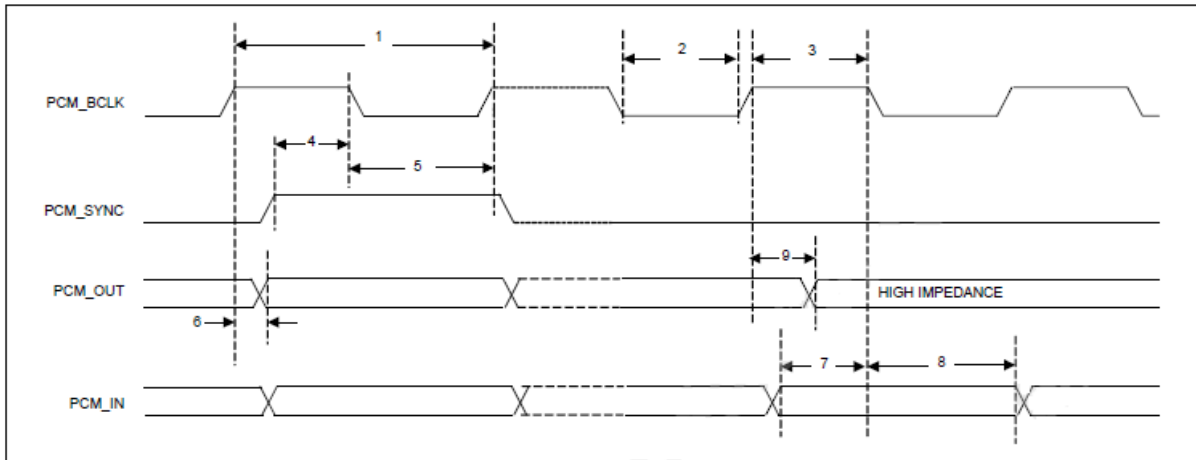


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

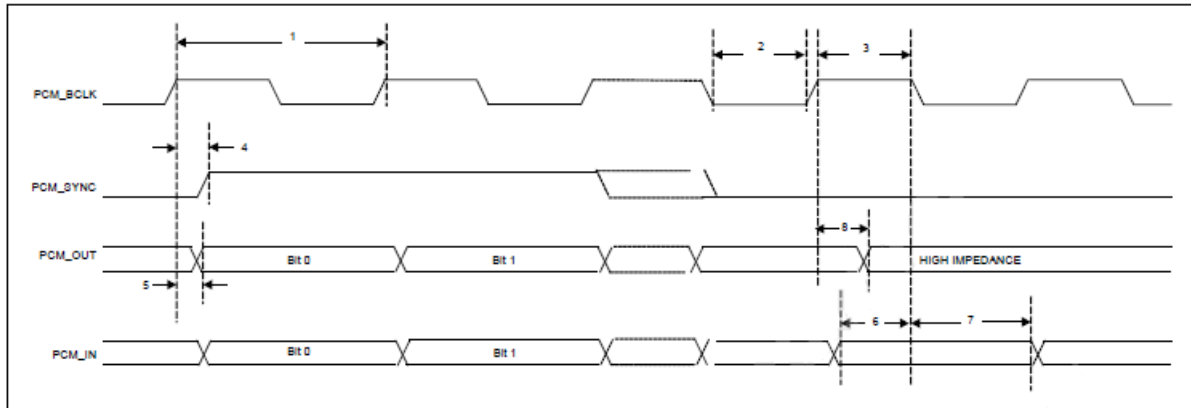


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

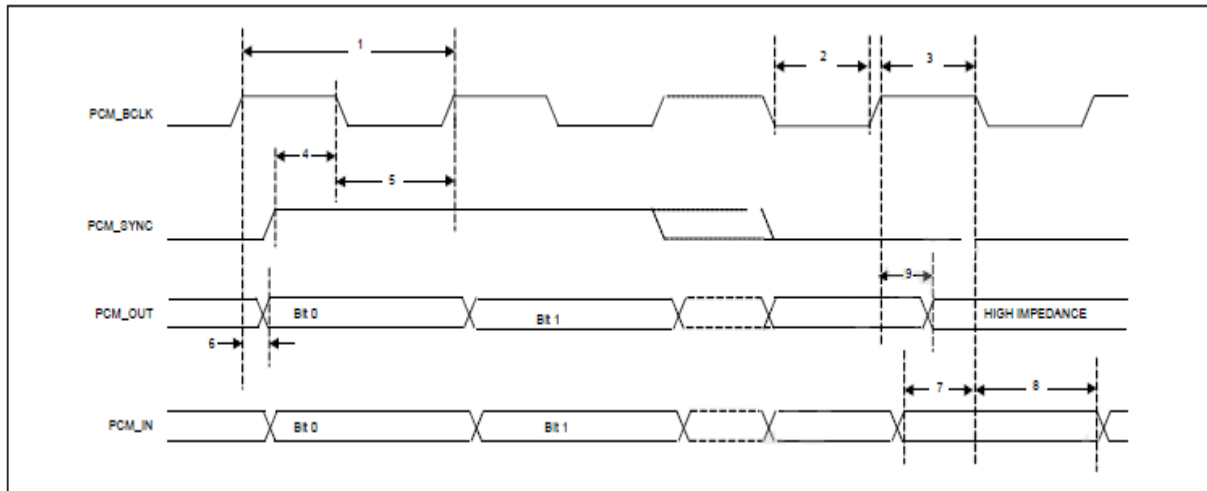


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

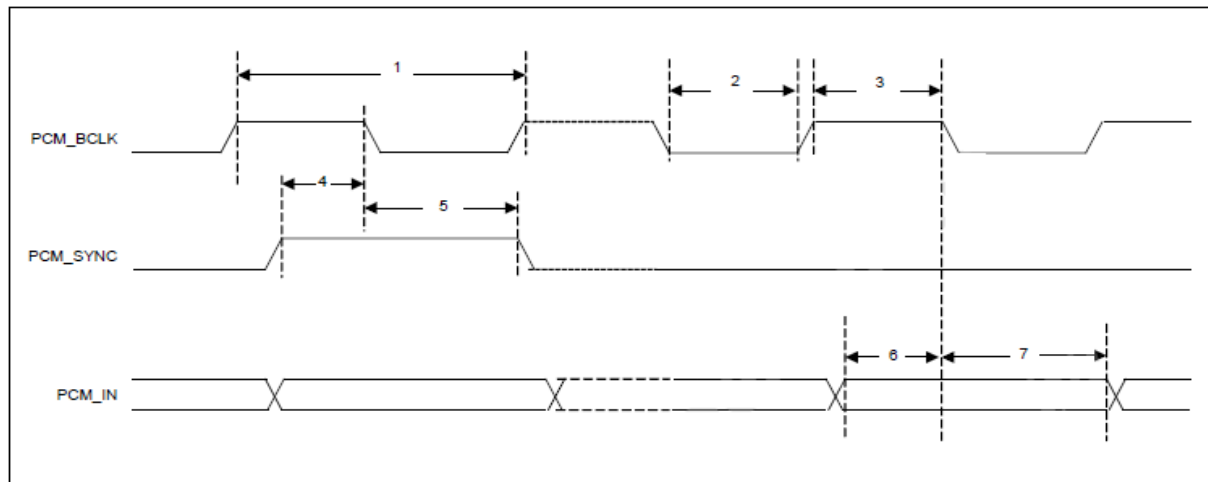


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

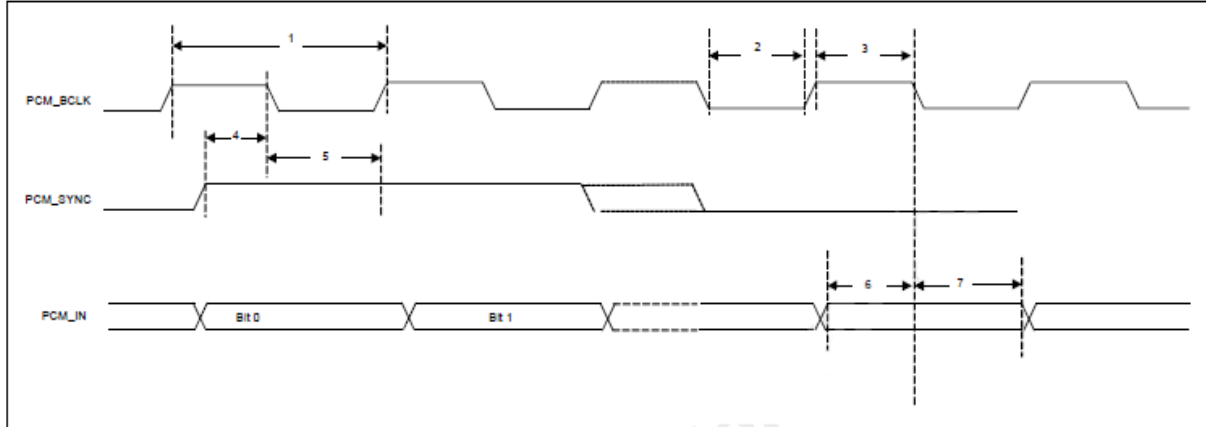


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.5 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

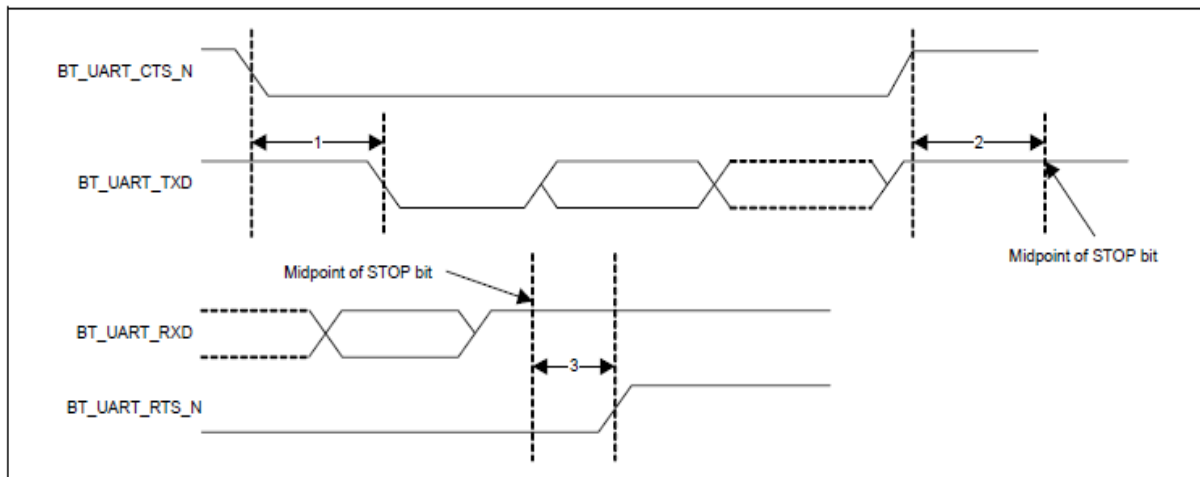
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

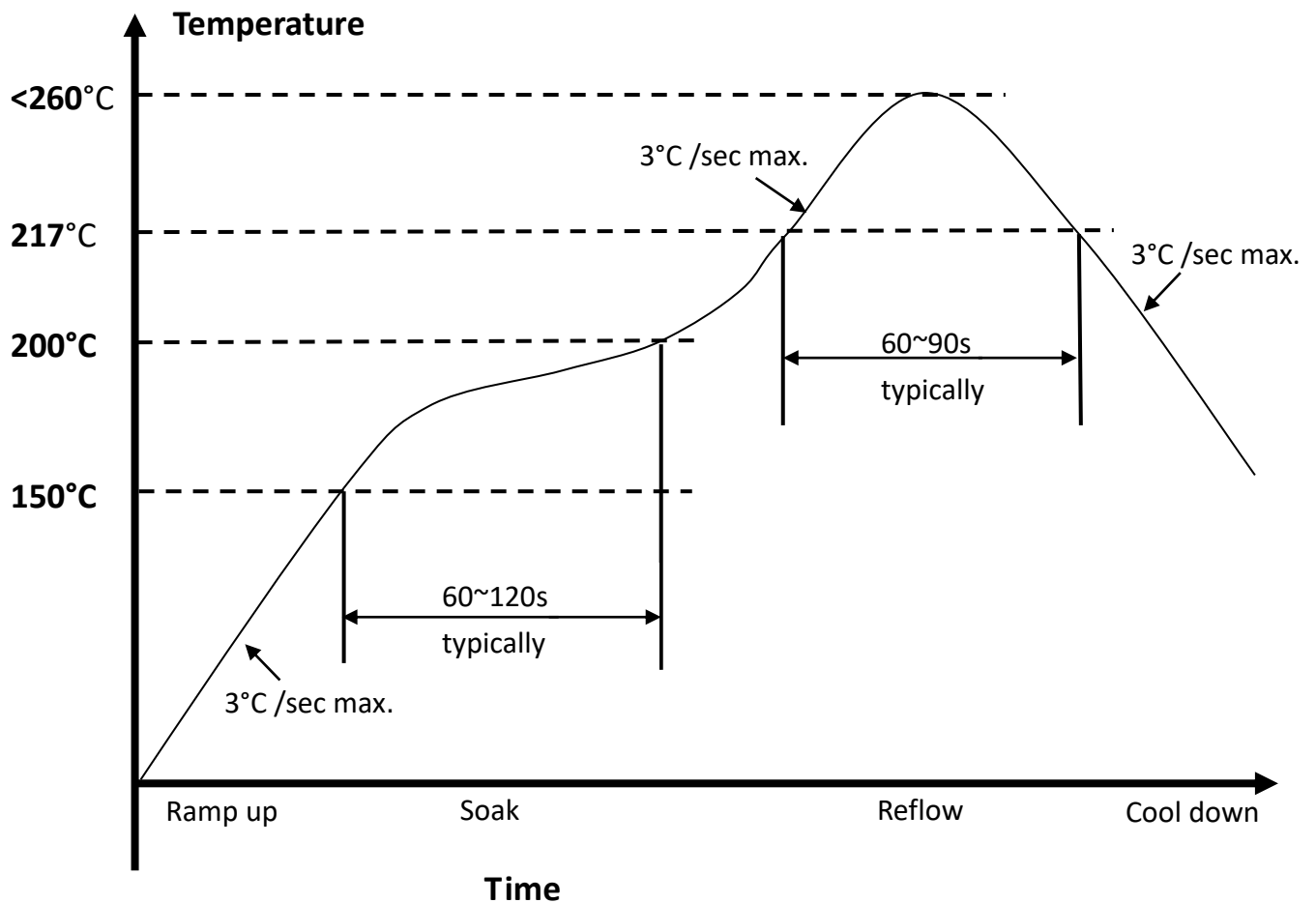
UART Timing



UART Timing Specifications

Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

9. Recommended Reflow Profile

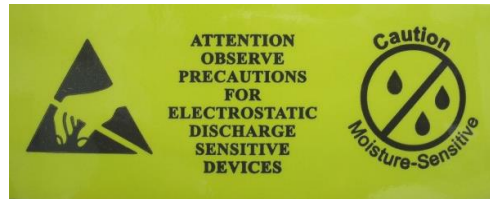


1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C (Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

10.1 Label

Label A → Anti-static and humidity notice



Label B → MSL caution / Storage Condition

	Caution	LEVEL
	This bag contains MOISTURE-SENSITIVE DEVICES	 If blank, see adjacent bar code label
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH) 2. Peak package body temperature: _____ °C If blank, see adjacent bar code label 3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be a) Mounted within: _____ hours of factory conditions If blank, see adjacent bar code label ≤30°C/60% RH, or b) Stored per J-STD-033 4. Devices require bake, before mounting, if: a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C b) 3a or 3b are not met 5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure Bag Seal Date: _____ If blank, see adjacent bar code label Note: Level and body temperature defined by IPC/JEDEC J-STD-020		

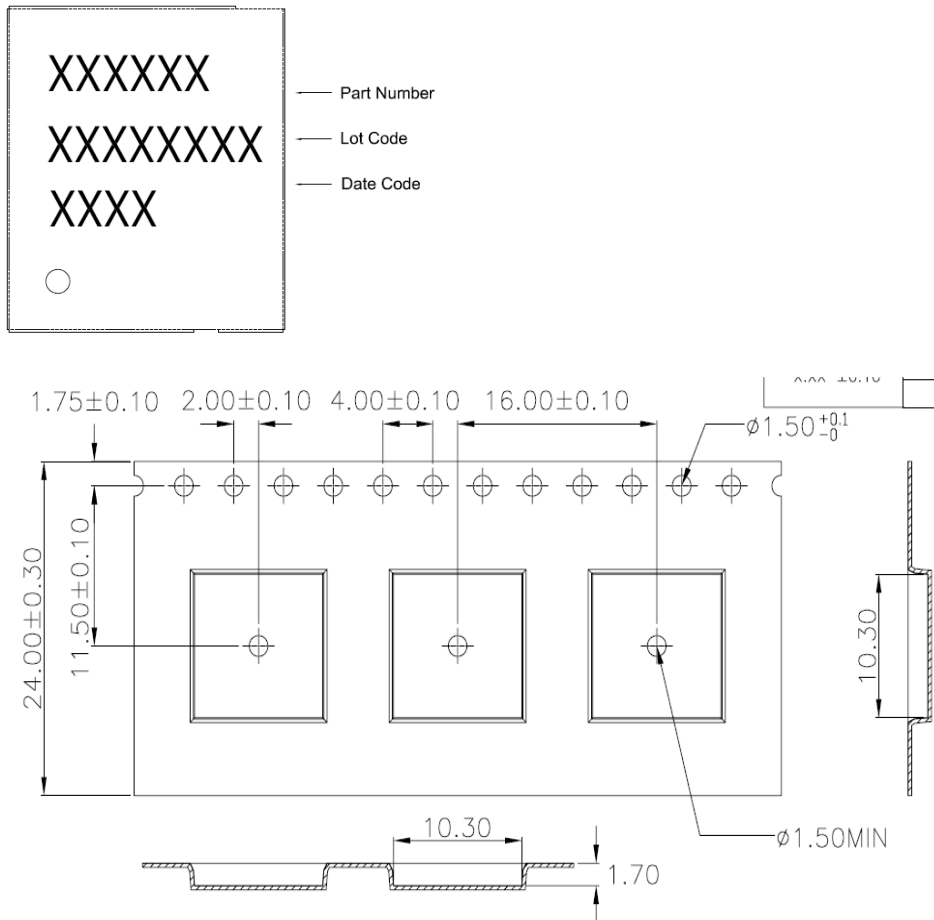
Label C → Inner box label .

PO:	
AMK DEVICE:	
PKG S/N:	 9PKGYYMDDNNNNN
Model Name:	 APXXXXXXXX (R3HF)
P/N:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Date Code:	 YYWW
Lot Code:	 XXXXXXXX

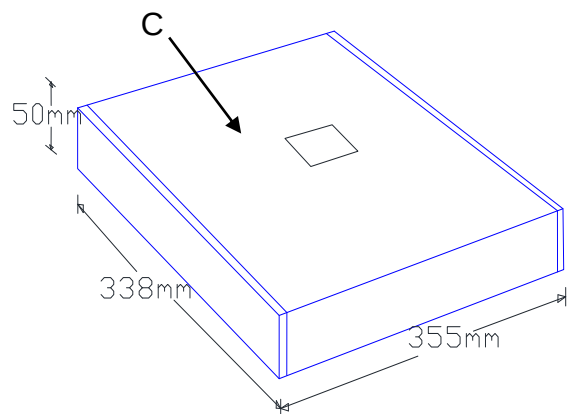
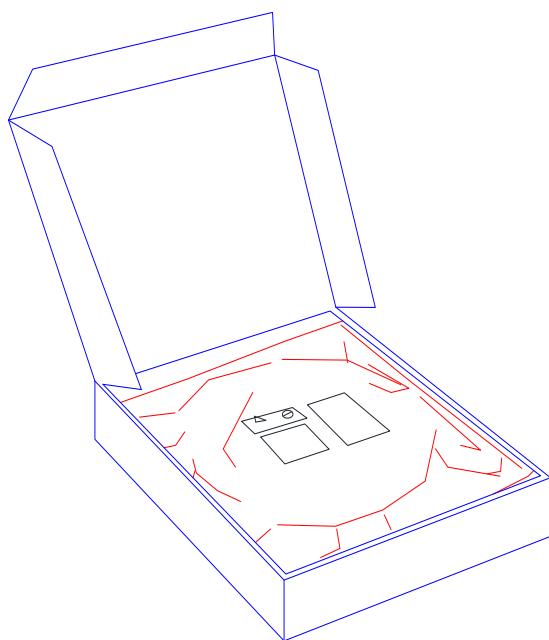
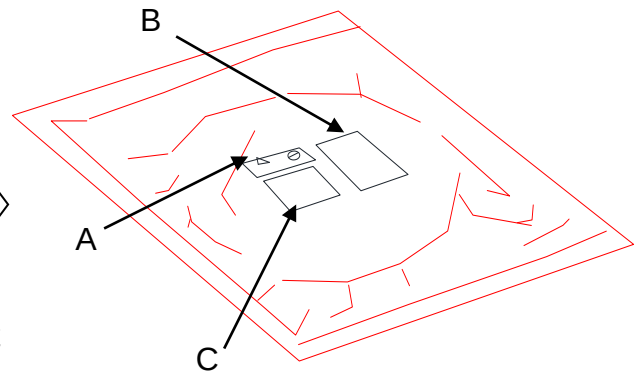
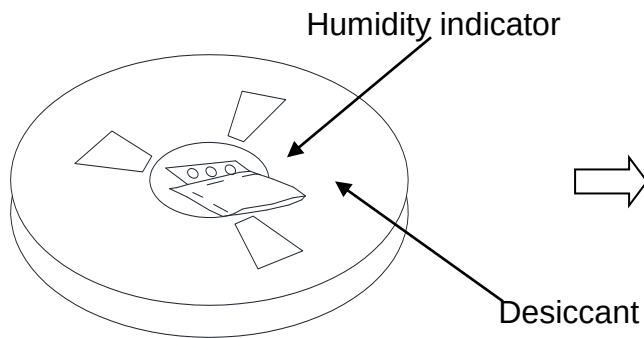
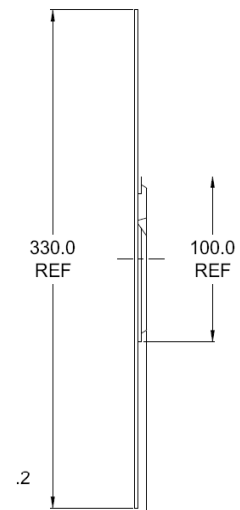
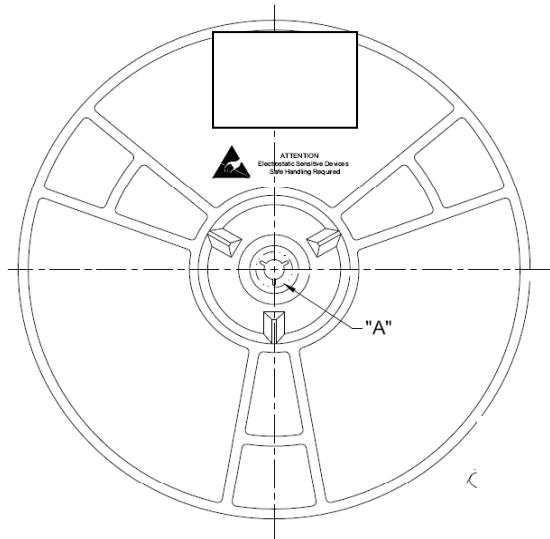
Label D → Carton box label .

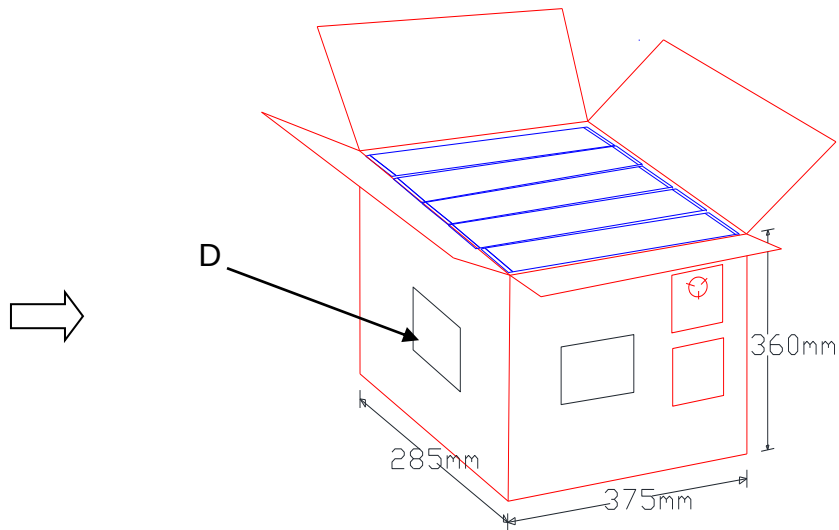
AMPAK Technology Inc.	
PO:	
AMK DEVICE:	
Model Name:	 APXXXXXXXX (R3HF)
Part No.:	 99X-XXX-XXXXR
Quantity:	 QQQQ
Lot D/C:	 XXXXXXXX YYWW QQQQ
Manufacture:	 YYYY/MM/DD

10.2 Dimension



1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness: 0.30 ± 0.05 mm.
6. Component load per 13" reel : 1000 pcs





10.3 MSL Level / Storage Condition



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL

4

If blank, see adjacent
bar code label

1. Calculated shelf life in sealed bag: 12 months at $<40^{\circ}\text{C}$ and $<90\%$ relative humidity (RH)
2. Peak package body temperature: 250 $^{\circ}\text{C}$
If blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
 - a) Mounted within: 72 hours of factory conditions
If blank, see adjacent bar code label
 $\leq 30^{\circ}\text{C}/60\% \text{ RH}$, or
 - b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
 - a) Humidity Indicator Card reads $>10\%$ for level 2a-5a devices or $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$
 - b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date: _____
If blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020